A Novel Three-Level Hysteresis Current Regulation Strategy for Three Phase Three-Level Inverters

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Abstract — This paper presents a new hysteresis current regulation strategy for the neutral point clamped (NPC) and flying capacitor (FC) three-level inverters. The strategy uses the measured average of the switched phase leg output voltage to adjust the controller hysteresis band as the load backemf varies, to maintain a near constant phase leg switching frequency. The phase leg switchings are then fine tuned to a fixed frequency clock to further improve frequency regulation. Next, the zero-crossings of the measured phase leg average voltages are used to select between positive and negative switched output voltage levels, so that only one hysteresis current regulator is required for the full inverter switched output voltage range. For the FC inverter, a state machine is then added to select between redundant switching states, to maintain balanced capacitor voltages. Finally, the controller is extended to a three phase system by subtracting the common mode interacting current from the total phase leg current error before making any switching decision. The resulting controller achieves a line-to-line harmonic performance that is very close to open-loop phase disposition (PD) Pulse Width Modulation, while retaining all of the dynamic benefits of hysteresis current regulation.

Keywords – Multilevel hysteresis control, three-level hysteresis current regulation, variable band, non-linear current control

I. INTRODUCTION

Multilevel converters are now well recognised as a most effective way of series cascading power switches to operate at higher voltage and power levels than individual switching devices can sustain. The two most common three level multilevel topologies are the neutral point clamped (NPC) [1][4] and the flying capacitor (FC) [2][3][4] inverters.

In many applications, these converters require closed loop current control, conventionally achieved using a linear regulator that feeds into a carrier-based modulator [5][6]. However, such regulators must be tuned to suit their load parameters, and their dynamic response can also be limited for higher power applications because of the relatively low switching frequency of such systems [6][7].

In contrast, non-linear current regulation strategies such as hysteresis are attractive because of their robustness to load parameter variations, fast dynamic response and inherent over current protection [6][7][8]. However, their switching frequency can vary significantly as operating conditions change, making it difficult to design output filters or calculate switching losses [6][8]. Also, switching interactions between the phase legs of a three-phase system often degrades the performance of a conventional hysteresis regulator [9][20].

The application of hysteresis current control (HCC) to multilevel inverters is even more challenging, with various approaches proposed such as multiband (MB), multi-offset (MO), time-based (TB) and space vector (SV) strategies [10]-[18]. MB and MO strategies use n-1 hysteresis bands for an n-level inverter to detect an out-of-band current error. However, they introduce DC tracking errors, and their multiple bands make it difficult to vary the band magnitude to maintain a constant switching frequency. TB strategies [10][11][14][15] solve this issue by using only one set of hysteresis bands and switching between voltage ranges when an out-of-band error is detected. However they are sensitive to noise at current zero crossings and have a poor dynamic response [6][10], SV strategies [16]-[18] use current error derivatives, per-phase leg comparators and a switching table to select the best voltage vector to directly correct a current phasor error. However inaccurate load back-emf estimation can cause the the wrong voltage vector to be selected, resulting in a harmonic performance that is typically poorer than open-loop PD modulation [16][17]. They also do not achieve exact constant switching frequency operation near the phase voltage polarity change [18], and interactions can still occur between phase leg switching events because of common mode currents [19].

This paper presents a new hysteresis regulation approach that overcomes these shortcomings. The strategy directly measures the average inverter switched output voltages, and uses these voltages to vary the hysteresis band magnitude to maintain a near constant switching frequency [20]. The zero-crossing of these voltages are then used to determine the switched output voltage polarity, so that only one hysteresis comparator is required per phase leg. Next, the hysteresis output is decoded into switching signals for the NPC, and further processed using a finite state machine for the FC to maintain a balanced voltage across the internal flying capacitor. Finally, the controller is extended to a three phase system by compensating for the common mode interacting current in the same way as has been done for two-level inverters [19][20]. The overall result is an almost constant switching frequency multilevel hysteresis regulator which has a harmonic performance that is very similar to the optimum open-loop PD PWM for a three level inverter [20].

II. OVERVIEW OF NPC AND FC MULTI-LEVEL INVERTERS

Fig. 1 shows the structure of a single phase leg of an NPC and FC inverter, feeding into a series RL impedance with an AC back-emf $E(t)$. The NPC inverter is formed by series
connecting two two-level phase legs, with their internal "outputs" clamped to the NP midpoint by series diodes. For the FC inverter, these clamping diodes are replaced by a flying capacitor. Both topologies can produce three switched output voltage levels, i.e. \( V(t) = 0, \pm V_{DC} \). Table I summarizes the relationship between the output voltage levels, the NPC switching signals and FC switching signals. Note that the NPC inverter ZERO state can only be achieved by turning on the middle two switches \( S_{1a}(t), S_{2a}(t) \), while the FC inverter ZERO state can be achieved by either of two switching combinations. This state redundancy can be used to adjust the modulating of this topology to maintain a balanced flying capacitor voltage even when PD PWM is used [4][21].

III. CONSTANT SWITCHING FREQUENCY HYSTERESIS

A. Variable Hysteresis Band for Three-level Inverter

From Fig. 1 the phase leg KVL load equation is

\[
V(t) = RI(t) + L \frac{dI(t)}{dt} + E(t)
\]

where \( V(t) = 0, \pm V_{DC} \) depending on the inverter state.

The load current can be split into fundamental \( I_f(t) \) and switching ripple \( I_s(t) \) components as:

\[
I(t) = I_f(t) + I_s(t)
\]

(2)

Recognising that the switching ripple voltage drop across \( L \) is much greater than across \( R \), (1) and (2) can be reduced to

\[
\frac{dI_s(t)}{dt} = \frac{V(t) - V_{avg}(t)}{L}
\]

(3)

where \( V_{avg}(t) = E(t) + L dI_f/dt \) is the fundamental voltage component of the phase leg switched output.

Fig. 2 illustrates the inverter switching process over a complete fundamental cycle with a fixed hysteresis band, showing how the switched output voltage varies between \( (0, V_{DC}) \) or \( (0, -V_{DC}) \), depending on the required output voltage polarity. During period \( t_1 \), Fig. 2 (i.e. a positive inverter output voltage), the inverter switched output voltage is \( +V_{DC} \), and the load current ramps \( 2I_h \) from \( I^* - I_h \) (\( I^* \) is the commanded current reference) to \( I^* + I_h \), during the period \( (T_1 - t_1) \), the inverter output voltage is 0 and the load current ramps back from \( I^* + I_h \) to \( I^* - I_h \). Similarly during period \( t_2 \) (i.e. a negative average inverter output voltage), the inverter switched output is \( -V_{DC} \) and the load current ramps \( 2I_h \) from \( I^* + I_h \) to \( I^* - I_h \), while during period \( (T_2 - t_2) \) the inverter output voltage is 0 and the current ramps back from \( I^* - I_h \) to \( I^* + I_h \).

Since \( V_{avg}(t) \) is almost constant between switching events, these switching times can be determined from (3) as:

\[
t_1 = \frac{2LI_h}{V_{DC} - V_{avg}(t)} \quad , \quad T_1 - t_1 = \frac{-2LI_h}{0 - V_{avg}(t)}
\]

(4a)

\[
t_2 = \frac{-2LI_h}{-V_{DC} - V_{avg}(t)} \quad , \quad T_2 - t_2 = \frac{2LI_h}{0 - V_{avg}(t)}
\]

(4b)

Removing \( t_1 \) and \( t_2 \) from (4a) and (4b) gives

\[
T_s = \frac{2LI_h V_{DC}}{V_{avg}(t) V_{DC} - V_{avg}(t)} \quad , \quad V_{avg}(t) = +ve
\]

(5a)

\[
T_s = \frac{-2LI_h V_{DC}}{-V_{avg}(t) V_{DC} + V_{avg}(t)} \quad , \quad V_{avg}(t) = -ve
\]

(5b)

From (5), an essentially constant switching frequency \( f_{sw} \) of approximately \( T_s = T_c = T = 1/f_{sw} \) can be achieved for both inverter output voltage polarities by making

\[
I_h = I_{h\_max} \left[ V_{avg}(t) / V_{DC} \right] \left[ 1 - V_{avg}(t) / V_{DC} \right] / \left[ V_{avg}(t) / V_{DC} \right]
\]

(6)

as \( V_{avg}(t) \) and the reference current \( I^* \) change.
The term $I_{h,\text{max}} = \frac{V_{DC}}{2f_{sw}}$ in (6) is the maximum hysteresis band magnitude, set to achieve a desired switching frequency based on the system parameters, while $|V_{\text{avg}}(t)/V_{DC}|$ is the absolute normalized value of the phase leg average voltage $V_{\text{avg}}(t)$. This voltage can be measured without delay on a switching cycle by cycle basis using a DSP capture/timer port, which records the instance of each inverter switching transition using a continuously cycling internal timer. The voltage is then calculated using [20]

$$
|V_{\text{avg}}(t)| = V_{DC} \frac{T_2 - T_1}{T_1 - T_1}
$$

where $T_1, T_2, T_3$ are the switching instances shown in Fig. 2.

B. Synchronization to a Fixed Reference Clock [20]

The stability of the switching frequency, and hence a better harmonic switching performance, can be further improved if the regulator switching is fine-tuned using current error zero-crossings to follow a fixed reference clock, as shown in Fig. 3. From this figure, if a time error $\delta t$ occurs between the current error zero-crossing and the reference clock, it can be corrected by trimming the hysteresis band using

$$
\delta_h = \frac{J_s \times \delta t}{T/2} = -J_s \times 2 f_{in} \times \delta t
$$

Hence the overall hysteresis band variation to maintain a constant switching frequency becomes

$$
I_{h,\text{new}} = \delta_h + I_h
$$

Because the current error zero-crossings occur essentially midway between the rising and falling edges of the inverter switched output (shown in Fig 2), they can be calculated by

$$
Z_1 = (T_1 + T_2)/2, \quad Z_2 = (T_2 + T_3)/2, \quad \text{etc}
$$

Since the switching times $T_1, T_2, T_3, \ldots$ have already been recorded by the DSP timer/capture port for the average inverter voltage calculation, no additional hardware detection circuitry is required to implement this refinement.

IV. IMPLEMENTATION OF VARIABLE BAND HYSTERESIS MODULATOR FOR THREE-LEVEL NPC AND FC VSI

Fig. 4 shows the circuitry required to implement the multilevel variable band hysteresis modulation system for one phase leg of a NPC and FC inverter. The circuit:

(a) Manages the hysteresis switching process and generates the NPC & FC inverter switching signals, and

(b) Detects the point of the output voltage polarity change.

A. Managing the Hysteresis Switching Process

The basic hysteresis operation is implemented using analog circuitry that subtracts the measured phase leg current from the target reference to create the current error. This error is then compared against the variable hysteresis bands set by (9), to create the switched output command $S_{a,\text{ref}}(t)$. The NPC decoding logic shown in Fig. 4(a) combines $S_{a,\text{ref}}(t)$ with the polarity selection signal $R_a(t)$ to create the switch gate signals. For the positive fundamental half cycle, where $R_a(t)$=1, $S_{a,\text{ref}}(t)$ toggles $S_{PD},l(t)$ to switch the phase leg between $+V_{DC}$ and 0V, while $S_{PD,2a}(t)$ is held ON.

For the negative fundamental half cycle, where $R_a(t)$=0, $S_{a,\text{ref}}(t)$ toggles $S_{PD,2a}(t)$ to switch the phase leg between 0V and $-V_{DC}$ while $S_{PD,1a}(t)$ is held OFF.

The FC decoding logic shown in Fig. 4(b) adds an additional finite state machine (FSM) that uses $S_{PD,1a}(t)$ and $S_{PD,2a}(t)$ to step through a “round robin” assignment of the redundant 0V switching states. This ensures a balanced voltage is maintained across the internal flying capacitor, as described in [21]. The logic of this FSM is shown in Fig 5, where it cycles the switched output through the sequence $+V_{DC} \rightarrow 0_1 \rightarrow +V_{DC} \rightarrow 0_2$ as $S_{PD,1a}(t)$ switches during the

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positive fundamental half cycle, and the sequence \(-V_{DC} \rightarrow 0_1 \rightarrow V_{DC} \rightarrow 0_2\) as \(S_{PD,2a}(t)\) switches during the negative fundamental half cycle.

Fig. 6(a) shows the current error compared against the variable hysteresis band, while Fig. 6(b) shows the resultant comparator switched output and its raw average value \(S_{a,OR,avg}(t)\). For the negative half of the fundamental, this average is level shifted by +1, since during this region the comparator zero output state selects the negative active output average is level shifted by +1, since during this region the

\[ V_{DC} \rightarrow 0_1 \rightarrow V_{DC} \rightarrow 0_2 \]

Fig. 7 illustrates this process, where it can be seen how the current error curves away from the upper hysteresis band because the inverter 0V output voltage does not adequately drive the current to follow the reference. The DSP recognises this situation, toggles \(R_a(t)\), the inverter output switches to \(-V_{DC}\), the current immediately ramps back to the upper hysteresis band and switching recommences. Fig. 8 confirms this response experimentally, where the phase leg switching is locked to the 5 kHz synchronising clock before the zero crossing, freewheels for a number of clock cycles as the output polarity nears zero and the current error does not hit a hysteresis boundary, and then recommences switching and rapidly resynchronises to the reference clock as the DSP reverses the commanded output voltage polarity.

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The DSP identifies when the average value of the switched output signal \(S_{a,OR,avg}(t)\) falls below a given modulation depth threshold (the threshold value was set experimentally to 20%, but the value is not particularly critical). This detection is coupled with knowledge of when a polarity change might be expected, based on the period of the current reference waveform. Together, the two events identify that a zero crossing event is about to happen.

Once in this region, the DSP now predicts when the next comparator OFF switching event should occur, on the basis that the switching frequency is essentially constant, and so
point, the delayed implementation of a near zero hysteresis band can cause short term high frequency switching, unless it is clamped to a minimum value [19]. The optimum clamp value is a tradeoff between excessive switching if it is too small, and a degraded harmonic performance because the switching frequency varies too much if it is too large. A minimum band of 20% was found to be an effective value.

V. IMPLEMENTATION IN A THREE PHASE SYSTEM

The system can be readily extended to a three-level three-phase system using three separate current regulators as follows. For each phase, the KVL load equation is:

\[ V_s(t) = L \frac{dI_s(t)}{dt} + RI_s(t) + E_s(t) + U_0(t), \quad x = a, b, c \]  

(12)

where \( U_0(t) \) is the load floating neutral point voltage.

The three-phase currents can be separated into non-interacting \( I_s \) and interacting \( \gamma(t) \) components as [19][20]:

\[ I_s(t) = I_s^* + \gamma(t), \quad x = a, b, c \]  

(13)

The interacting current term part of (12) is now equated to the negative of the neutral point voltage \( U_0(t) \), viz

\[ L \frac{d\gamma(t)}{dt} + R\gamma(t) = -U_0(t) \]  

(14)

Eqn. (12) then can be simplified using (13) and (14), to give:

\[ V_s(t) = L \frac{dI_s^*(t)}{dt} + RI_s^*(t) + E_s(t), \quad x = a, b, c \]  

(15)

With this reduction, (15) is identical to (1) for each individual phase current, which allows the previously developed single phase leg three-level variable hysteresis band concepts to be directly applied to the three phase system.

The interacting current can be calculated by recognising that the sums of the three phase currents and backemf voltages for a balanced three phase system are always zero. Hence summing (12) across all three phases results in:

\[ U_0(t) = \frac{1}{3}[V_a(t) + V_b(t) + V_c(t)] \]  

(16)

Since the resistive voltage drop \( R\gamma(t) \) in (14) will always be small compared to the derivative term, the common mode interacting current can be adequately calculated using:

\[ \gamma(t) = -\frac{1}{L} \int U_0(t) dt = \frac{1}{3L} \int [V_a(t) + V_b(t) + V_c(t)] dt \]  

(17)

It is then subtracted from the measured current before proceeding to the hysteresis comparison process.

VI. EXPERIMENTAL SYSTEM

Fig. 9 shows how the new hysteresis current regulator was constructed for three phase three-level NPC and FC inverters with parameters as listed in Table II The load currents are measured by LEM LA-100P Hall Effect transducers. Op-amp summing junctions are then used to calculate the phase current errors and subtract the common mode interacting current. The resultant non-interacting errors feed into variable threshold analogue comparators whose outputs create the three-phase hysteresis switching signals \( S_{a,b,c}(t) \), \( S_{a,b,c}(t) \), \( S_{a,b,c}(t) \). The NPC and FC decoding logic and associated dead-time delay logic is then implemented in a MAX II CPLD, to create the inverter device output switching signals. The CPLD also generates the modified switching signals \( S_{a,b,c}(t) \), \( S_{a,b,c}(t) \), \( S_{a,b,c}(t) \) which feed into the timer/capture ports of the controlling DSP to trigger the average switching voltage calculation using (7). With this voltage, the DSP calculates the required variable hysteresis bands for each phase leg using (6) and (8), and outputs them through a DAC to create the variable hysteresis band threshold levels for the analog comparators.

The common mode interacting current is calculated using an additional DAC output from the DSP, scaled to match the measured positive bus voltage. This output (and its inverse) are processed through a multiplexer driven by the converter phase leg switching states, to create scaled representations of the phase leg three-level switched voltages. Next, these voltages are summed, integrated and scaled using op-amp analog circuitry as per (17), to create the common mode interacting current. Finally, this current is subtracted from the measured current to create the non-interacting current errors for the variable band hysteresis comparison.

VII. SINGLE PHASE EXPERIMENTAL RESULTS

Fig. 10 shows the essentially constant switching frequency achieved by this scheme, with only a small residual frequency fluctuation. This is caused by a one switching cycle delay in the calculation of \( V_{avg}(t) \) using (7), which introduces a slight error in the variable hysteresis band calculation (6).

Figs. 11(a)(b) show experimental results for the new controller operating with both fixed and variable hysteresis bands to regulate the current into a three-level NPC inverter. Fig. 11(c)(d) show experimental results with both fixed and

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overall DC Link Voltage</td>
<td>((2V_{dc}))</td>
</tr>
<tr>
<td>Filter Inductance (L)</td>
<td>18 mH</td>
</tr>
<tr>
<td>Output Resistance (R)</td>
<td>0.5 Ω</td>
</tr>
<tr>
<td>Switching Frequency (f_s)</td>
<td>2500 Hz</td>
</tr>
<tr>
<td>Fundamental Frequency (f_f)</td>
<td>50Hz</td>
</tr>
</tbody>
</table>
variable hysteresis bands to regulate the current into one phase of a three-level FC inverter. The figures show excellent output current tracking capability under both fixed and variable hysteresis band operation without any sign of DC tracking error. Also, it can be seen in these figures how the current error loops back from the hysteresis boundary without actually hitting it during the level change transition, while the controller smoothly continues switching after the polarity change. The figures also show a clear three-level switched phase voltage, especially at the zero voltage transition points. This confirms the effectiveness of the level selection strategy based on the prediction of the average voltage zero-crossing, which avoids the erroneous polarity transitions that are always constrained between two successive voltage levels at any point in time, although with some leakage because of hysteresis band clamping during voltage level transitions, as shown in Fig 8. Figs. 15(b) and 16(b) confirm this result, showing harmonic line voltage spectra with no common mode carrier harmonic in the line-line voltage as anticipated from the single phase results.

VIII. THREE PHASE EXPERIMENTAL RESULTS

Experimental results are respectively presented in Figs. 13 and 15 for the NPC inverter, and Figs 14 and 16 for the FC inverter, for a pulse ratio of 50 (f_s = 2500Hz, f_o = 50Hz). Fig. 15(a) and Fig. 16(a) show the distinctive pattern of PD modulation in the five-level line-to-line voltages (switching always constrained between two successive voltage levels at any point in time), although with some leakage because of hysteresis band clamping during voltage level transitions, as shown in Fig 8. Figs. 15(b) and 16(b) confirm this result, showing harmonic line voltage spectra with no common mode carrier harmonic in the line-line voltage as anticipated from the single phase results.

Fig 17(a)(b) shows the system’s transient response achieved for a 100% step-up change in reference current for the NPC and FC inverters, which confirms that the variable hysteresis band addition has not compromised the excellent
dynamic response of the conventional hysteresis control [6]. Note also how the variable band fluctuation increases after the transient due to the resultant increase in load back-emf.

IX. CONCLUSION

This paper has presented a new variable band hysteresis regulation strategy for a three level NPC and FC multilevel inverter. The strategy uses the averaged voltages of the phase leg switched outputs to vary the hysteresis bands so as to maintain a near constant phase leg switching frequency. The same average output voltages are then used to detect the polarity change of each phase leg voltage, allowing their phase leg switchings to be controlled using a single hysteresis comparator (in conjunction with some simple combination logic). These improvements significantly improve the performance of the system compared to previous multilevel hysteresis approaches. Finally, the common mode interacting current for a three phase system is removed before hysteresis control of each phase leg, to achieve high quality, high performance current regulation with a harmonic performance that is very close to open loop PD PWM.

X. REFERENCES


Three Phase Currents (A)

Variable Band & Current Error (A)

Three Phase Voltages (V)

Experimental - Three Phase NPC Results

Experimental - Three Phase FC Results

Fig. 13: Experimental results of the proposed controller for three-level NPC inverter ($f_{sw}/f_o=50$, modulation depth=0.9). Three phase (a) output currents (b) current errors and variable bands (c) phase voltages.

Fine-tuned Variable Band

Experimental - Three Phase Line Voltages

Experimental - Three Phase FC Line Voltages (V)

Fig. 14: Experimental results of the proposed controller for three-level FC inverter ($f_{sw}/f_o=50$, modulation depth=0.9). Three phase (a) output currents (b) current errors and variable bands (c) phase voltages.

Experimental – NPC Line Voltage Harmonic Spectrum

Experimental – FC Line Voltage Harmonic Spectrum

Fig. 15: Experimental results of three phase NPC (a) line voltages (b) Line to line harmonic spectrum ($f_{sw}/f_o=50$, modulation depth=0.9).

Fig. 16: Experimental results of three phase FC (a) line voltages (b) Line to line harmonic spectrum ($f_{sw}/f_o=50$, modulation depth=0.9).
Fig. 17: Experimental transient operation of the proposed three-level hysteresis current regulator showing output currents, current errors and variable hysteresis bands - 100% commanded step change in current (a) NPC inverter (b) FC inverter


