A Novel Three-Level Hysteresis Current Regulation Strategy for Three Phase Three-Level Inverters

R. Davoodnezhad, D. G. Holmes, B. P. McGrath
School of Electrical and Computer Engineering, RMIT University
Melbourne Australia

Abstract — This paper presents a new hysteresis current regulation strategy for the neutral point clamped (NPC) and flying capacitor (FC) three-level inverters. The strategy uses the measured average of the switched phase leg output voltage to adjust the controller hysteresis band as the load backemf varies, to maintain a near constant phase leg switching frequency. The phase leg switchings are then fine tuned to a fixed frequency clock to further improve frequency regulation. Next, the zero-crossings of the measured phase leg average voltages are used to select between positive and negative switched output voltage levels, so that only one hysteresis current regulator is required for the full inverter switched output voltage range. For the FC inverter, a state machine is then added to select between redundant switching states, to maintain balanced capacitor voltages. Finally, the controller is extended to a three phase system by subtracting the common mode interacting current from the total phase leg current error before making any switching decision. The resulting controller achieves a line-to-line harmonic performance that is very close to open-loop phase disposition (PD) Pulse Width Modulation, while retaining all of the dynamic benefits of hysteresis current regulation.

Keywords – Multilevel hysteresis control, three-level hysteresis current regulation, variable band, non-linear current control

I. INTRODUCTION

Multilevel converters are now well recognised as a most effective way of series cascading power switches to operate at higher voltage and power levels than individual switching devices can sustain. The two most common three level multilevel topologies are the neutral point clamped (NPC) [1][4] and the flying capacitor (FC) [2][3][4] inverters.

In many applications, these converters require closed loop current control, conventionally achieved using a linear regulator that feeds into a carrier-based modulator [5][6]. However, such regulators must be tuned to suit their load parameters, and their dynamic response can also be limited for higher power applications because of the relatively low switching frequency of such systems [6][7].

In contrast, non-linear current regulation strategies such as hysteresis are attractive because of their robustness to load parameter variations, fast dynamic response and inherent over current protection [6][7][8]. However, their switching frequency can vary significantly as operating conditions change, making it difficult to design output filters or calculate switching losses [6][8]. Also, switching interactions between the phase legs of a three-phase system often degrades the performance of a conventional hysteresis regulator [9][20].

The application of hysteresis current control (HCC) to multilevel inverters is even more challenging, with various approaches proposed such as multiband (MB), multi-offset (MO), time-based (TB) and space vector (SV) strategies [10]-[18]. MB and MO strategies use n-1 hysteresis bands for an n-level inverter to detect an out-of-band current error. However, they introduce DC tracking errors, and their multiple bands make it difficult to vary the band magnitude to maintain a constant switching frequency. TB strategies [10][11][14][15] solve this issue by using only one set of hysteresis bands and switching between voltage ranges when an out-of-band error is detected. However they are sensitive to noise at current zero crossings and have a poor dynamic response [6][10]. SV strategies [16]-[18] use current error derivatives, per-phase leg comparators and a switching table to select the best voltage vector to directly correct a current phasor error. However inaccurate load back-emf estimation can cause the the wrong voltage vector to be selected, resulting in a harmonic performance that is typically poorer than open-loop PD modulation [16][17]. They also do not achieve exact constant switching frequency operation near the phase voltage polarity change [18], and interactions can still occur between phase leg switching events because of common mode currents [19].

This paper presents a new hysteresis regulation approach that overcomes these shortcomings. The strategy directly measures the average inverter switched output voltages, and uses these voltages to vary the hysteresis band magnitude to maintain a near constant switching frequency [20]. The zero-crossing of these voltages are then used to determine the switched output voltage polarity, so that only one hysteresis comparator is required per phase leg. Next, the hysteresis output is decoded into switching signals for the NPC, and further processed using a finite state machine for the FC to maintain a balanced voltage across the internal flying capacitor. Finally, the controller is extended to a three phase system by compensating for the common mode interacting current in the same way as has been done for two-level inverters [19][20]. The overall result is an almost constant switching frequency multilevel hysteresis regulator which has a harmonic performance that is very similar to the optimum open-loop PD PWM for a three level inverter [20].

II. OVERVIEW OF NPC AND FC MULTI-LEVEL INVERTERS

Fig. 1 shows the structure of a single phase leg of an NPC and FC inverter, feeding into a series RL impedance with an AC back-emf $E(t)$. The NPC inverter is formed by series

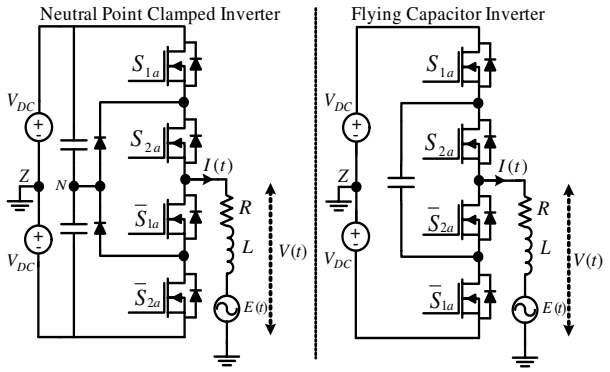

Fig. 1: Topology of single phase leg NPC (left) and FC (right) inverter.

connecting two two-level phase legs, with their internal "outputs" clamped to the NP midpoint by series diodes. For the FC inverter, these clamping diodes are replaced by a flying capacitor. Both topologies can produce three switched output voltage levels, i.e $V(t) = 0, \pm V_{DC}$. Table I summarizes the relationship between the output voltage levels, the NPC switching signals and FC switching signals. Note that the NPC inverter ZERO state can only be achieved by turning on the middle two switches $(\bar{S}_{1a}(t), S_{2a}(t))$, while the FC inverter ZERO state can be achieved by either of two switching combinations. This state redundancy can be used to adjust the modulation of this topology to maintain a balanced flying capacitor voltage even when PD PWM is used[4][21].

III. Constant Switching Frequency Hysteresis

A. *Variable Hysteresis Band for Three-level Inverter*

From Fig. 1 the phase leg KVL load equation is

$$V(t) = RI(t) + L\frac{dI(t)}{dt} + E(t) \tag{1}$$

where $V(t) = 0, \pm V_{DC}$ depending on the inverter state.

The load current can be split into fundamental $I_f(t)$ and switching ripple $I_r(t)$ components as:

$$I(t) = I_f(t) + I_r(t) \tag{2}$$

Recognising that the switching ripple voltage drop across L is much greater than across R, (1) and (2) can be reduced to

$$\frac{dI_r(t)}{dt} = \frac{V(t) - V_{avg}(t)}{L} \tag{3}$$

where $V_{avg}(t) = E(t) + L\,dI_f/dt$ is the fundamental voltage component of the phase leg switched output.

Fig. 2 illustrates the inverter switching process over a complete fundamental cycle with a fixed hysteresis band, showing how the switched output voltage varies between $(0, +V_{DC})$ or $(0, -V_{DC})$, depending on the required output voltage polarity. During period t_{1+} in Fig. 2 (i.e. a positive inverter output voltage), the inverter switched output voltage is $+V_{DC}$, and the load current ramps $2I_h$ from $I^* - I_h$ (I^* is the commanded current reference) to $I^* + I_h$. During the period $(T_+ - t_{1+})$, the inverter output voltage is 0 and the load current ramps back from $I^* + I_h$ to $I^* - I_h$. Similarly during period t_{1-} (i.e. a negative average inverter output voltage), the inverter switched output is $-V_{DC}$ and the load current ramps $2I_h$ from $I^* + I_h$ to $I^* - I_h$, while during period $(T_- - t_{1-})$ the inverter output voltage is 0 and the current ramps back from $I^* - I_h$ to $I^* + I_h$.

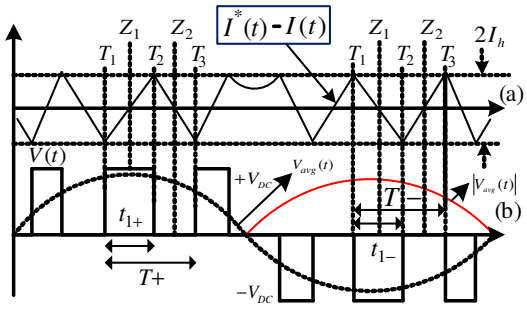

Fig. 2: Three-level hysteresis current regulation process (a) View of reference and actual current, (b) One fundamental cycle of the three-level switched and average output voltage. Note that the switching frequency is artificially low to better observe the switching processes.

Since $V_{avg}(t)$ is almost constant between switching events, these switching times can be determined from (3) as:

$$t_{1+} = \frac{2LI_h}{V_{DC} - V_{avg}(t)} \quad , \quad T_+ - t_{1+} = \frac{-2LI_h}{0 - V_{avg}(t)} \tag{4a}$$

$$t_{1-} = \frac{-2LI_h}{-V_{DC} - V_{avg}(t)} \quad , \quad T_- - t_{1-} = \frac{2LI_h}{0 - V_{avg}(t)} \tag{4b}$$

Removing t_{1+} and t_{1-} from (4a) and (4b) gives

$$T_+ = \frac{2LI_hV_{DC}}{V_{avg}(t)\{V_{DC} - V_{avg}(t)\}} \quad , \quad V_{avg}(t) = +ve \tag{5a}$$

$$T_- = \frac{2LI_hV_{DC}}{-V_{avg}(t)\{V_{DC} + V_{avg}(t)\}} \quad , \quad V_{avg}(t) = -ve \tag{5b}$$

From (5), an essentially constant switching frequency f_{sw} of approximately $T_+ = T_- = T = 1/f_{sw}$ can be achieved for both inverter output voltage polarities by making

$$I_h = I_{h\_\max}\left|V_{avg}(t)/V_{DC}\right|\left(1 - \left|V_{avg}(t)/V_{DC}\right|\right) \tag{6}$$

as $V_{avg}(t)$ and the reference current I^* change.

TABLE I: Switching states of single leg NPC, FC inverter.

Gate Signals S_{1a}, S_{2a} (NPC)	Output Voltage Level (NPC)	Gate Signals S_{1a}, S_{2a} (FC)	Output Voltage Level (FC)
S1: (1,1)	$+V_{DC}$	S1: (1,1)	$+V_{DC}$
S2: (0,0)	$-V_{DC}$	S2: (0,0)	$-V_{DC}$
S3: (0,1)	0	S3: (0,1)	0_1
S4: (1,0)	Hi Z	S4: (1,0)	0_2

The term $I_{h\_\max} = V_{DC} / 2Lf_{sw}$ in (6) is the maximum hysteresis band magnitude, set to achieve a desired switching frequency based on the system parameters, while $\left|V_{avg}(t)/V_{DC}\right|$ is the absolute normalized value of the phase leg average voltage $V_{avg}(t)$. This voltage can be measured without delay on a switching cycle by cycle basis using a DSP capture/timer port, which records the instance of each inverter switching transition using a continuously cycling internal timer. The voltage is then calculated using [20]

$$\left|V_{avg}(t)\right| = V_{DC}\left(\frac{T_2 - T_1}{T_3 - T_1}\right) \tag{7}$$

where T_1, T_2, T_3 are the switching instances shown in Fig. 2.

B. *Synchronization to a Fixed Reference Clock [20]*

The stability of the switching frequency, and hence a better harmonic switching performance, can be further improved if the regulator switching is fine-tuned using current error zero-crossings to follow a fixed reference clock, as shown in Fig. 3. From this figure, if a time error δt occurs between the current error zero-crossing and the reference clock, it can be corrected by trimming the hysteresis band using

$$\delta I_h = -\frac{I_h \times \delta t}{T/2} = -I_h \times 2 f_{sw} \times \delta t \tag{8}$$

Hence the overall hysteresis band variation to maintain a constant switching frequency becomes

$$I_{h,new} = \delta I_h + I_h \tag{9}$$

Because the current error zero-crossings occur essentially midway between the rising and falling edges of the inverter switched output (shown in Fig 2), they can be calculated by

$$Z_1 \approx (T_1 + T_2)/2\,,\quad Z_2 \approx (T_2 + T_3)/2\,,\ \text{etc} \tag{10}$$

Since the switching times $T_1, T_2, T_3 \ldots$ have already been recorded by the DSP timer/capture port for the average inverter voltage calculation, no additional hardware detection circuitry is required to implement this refinement.

IV. Implementation of Variable Band Hysteresis Modulator for Three-Level NPC and FC VSI

Fig. 4 shows the circuitry required to implement the multilevel variable band hysteresis modulation system for one phase leg of a NPC and FC inverter. The circuit:

(a) Manages the hysteresis switching process and generates the NPC & FC inverter switching signals, and
(b) Detects the point of the output voltage polarity change.

A. *Managing the Hysteresis Switching Process*

The *basic hysteresis operation* is implemented using analog circuitry that subtracts the measured phase leg current from the target reference to create the current error. This error is then compared against the variable hysteresis bands set by (9), to create the switched output command $S_{a,tot}(t)$.

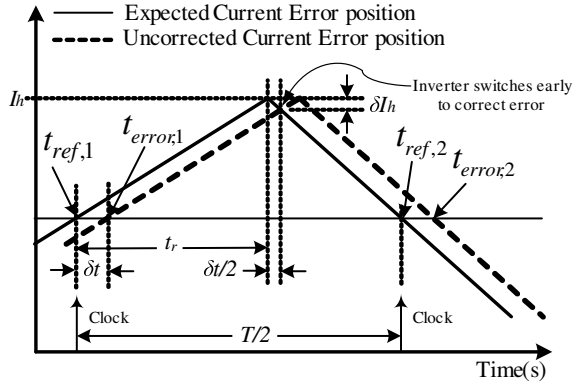

Fig. 3: Fine tuning variable band hysteresis regulation using current zero crossing error

The *NPC decoding logic* shown in Fig. 4(a) combines $S_{a,tot}(t)$ with the polarity selection signal $R_a(t)$ to create the switch gate signals. For the positive fundamental half cycle, where $R_a(t) = 1$, $S_{a,tot}(t)$ toggles $S_{PD,1a}(t)$ to switch the phase leg between $+V_{DC}$ and 0V, while $S_{PD,2a}(t)$ is held ON. For the negative fundamental half cycle, where $R_a(t) = 0$, $S_{a,tot}(t)$ toggles $S_{PD,2a}(t)$ to switch the phase leg between 0V and $-V_{DC}$ while $S_{PD,1a}(t)$ is held OFF.

The *FC decoding logic* shown in Fig. 4(b) adds an additional finite state machine (FSM) that uses $S_{PD,1a}(t)$ and $S_{PD,2a}(t)$ to step through a "round robin" assignment of the redundant 0V switching states. This ensures a balanced voltage is maintained across the internal flying capacitor, as described in [21]. The logic of this FSM is shown in Fig 5, where it cycles the switched output through the sequence $+V_{DC} \rightarrow 0_1 \rightarrow +V_{DC} \rightarrow 0_2$ as $S_{PD,1a}(t)$ switches during the

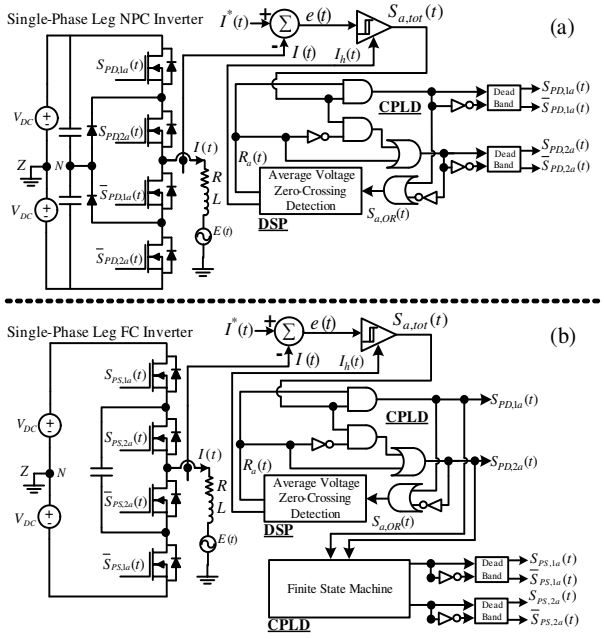

Fig. 4: (a) Combinational logic circuit to decode the total switching signal into gate switching signals for NPC (b) combinational logic circuit and FSM to decode the total switching signal into gate switching signals for FC VSI

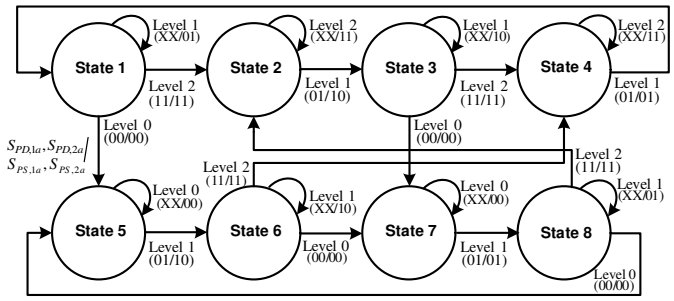

Fig. 5: Finite State machine diagram used to utilize the redundant zero state for the modulation of FC inverter

positive fundamental half cycle, and the sequence $-V_{DC} \rightarrow 0_1 \rightarrow -V_{DC} \rightarrow 0_2$ as $S_{PD,2a}(t)$ switches during the negative fundamental half cycle.

Fig. 6(a) shows the current error compared against the variable hysteresis band, while Fig. 6(b) shows the resultant comparator switched output and its raw average value $S_{a,tot,avg}(t)$. For the negative half of the fundamental, this average is level shifted by +1, since during this region the comparator zero output state selects the negative active output of $-V_{DC}$, rather than 0V. $S_{a,tot,avg}(t)$ is thus unsuitable for the variable hysteresis band calculation, since (6) requires the absolute average of the switched comparator output. To solve this problem, additional inverter/OR logic is added to create the switched signal $S_{a,OR}(t)$ shown in Fig. 6(c), which has the required absolute value average waveshape as shown in the figure. This signal feeds into the DSP comparator input for the average voltage calculation using (7).

Figs. 6(d) shows the VSI switching signals for the NPC inverter, with the characteristic pattern of PD PWM where each switch only operates for half the fundamental period. Fig 6(e) shows the VSI switching signals for the FC inverter, where the FSM round robin assignment of the zero state has made each switch continuously switch over the entire fundamental cycle, while still retaining the harmonic benefits of the PD PWM implementation.

B. Detecting the Output Voltage Polarity Change

As the commanded current reference changes sign, the inverter output has to change from switching between $+V_{DC}$ and 0V, to switching between 0V and $-V_{DC}$. The DSP manages this process by toggling $R_a(t)$, once it detects the impending polarity change using a two stage process.

Firstly, the DSP identifies when the average value of the switched output signal $S_{a,ORavg}(t)$ falls below a given modulation depth threshold (the threshold value was set experimentally to 20%, but the value is not particularly critical). This detection is coupled with knowledge of when a polarity change might be expected, based on the period of the current reference waveform. Together, the two events identify that a zero crossing event is about to happen.

Once in this region, the DSP now predicts when the next comparator OFF switching event should occur, on the basis that the switching frequency is essentially constant, and so

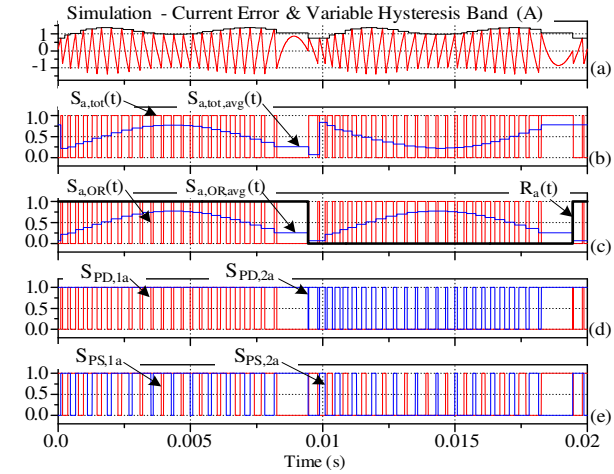

Fig. 6: (a) Phase current error and variable hysteresis band (b) hysteresis switching signals and its fundamental component (c) modified hysteresis switching signals and its fundamental component (d) NPC VSI switching signals (inputs to FSM) (e) FC VSI switching signals (outputs from FSM)

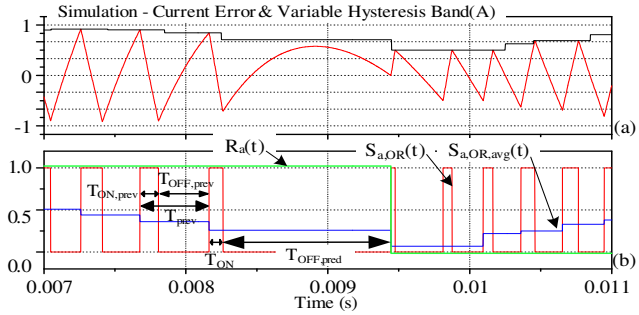

Fig. 7: Zoomed view of (a) phase current error and variable hysteresis band (b) modified hysteresis switching signals and its fundamental component

$$T_{OFF,pred} \approx T_{OFF,prev} + T_{ON} \tag{11}$$

If the switching event does not occur in this time, the DSP assumes that an output polarity change is required, and toggles $R_a(t)$.

Fig 7 illustrates this process, where it can be seen how the current error curves away from the upper hysteresis band because the inverter 0V output voltage does not adequately drive the current to follow the reference. The DSP recognises this situation, toggles $R_a(t)$, the inverter output switches to $-V_{DC}$, the current immediately ramps back to the upper hysteresis band and switching recommences. Fig. 8 confirms this response experimentally, where the phase leg switching is locked to the 5 kHz synchronising clock before the zero crossing, freewheels for a number of clock cycles as the output polarity nears zero and the current error does not hit a hysteresis boundary, and then recommences switching and rapidly resynchronises to the reference clock as the DSP reverses the commanded output voltage polarity.

It can be seen also in Fig 8 how the variable hysteresis band in practice is clamped to a minimum value rather than reducing to near zero at the polarity change. This is done because the average voltage measurement of (7), and hence the variable hysteresis band calculation, is always lagging the switching by one cycle. Just after the voltage zero crossing

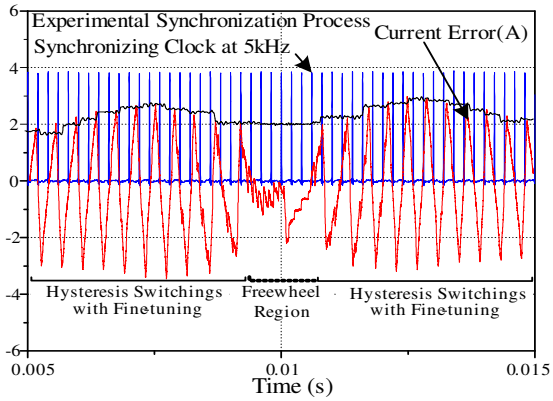

Fig. 8: Experimental response at fundamental voltage zero crossing (Modulation Depth = 0.9)

point, the delayed implementation of a near zero hysteresis band can cause short term high frequency switching, unless it is clamped to a minimum value [19]. The optimum clamp value is a tradeoff between excessive switching if it is too small, and a degraded harmonic performance because the switching frequency varies too much if it is too large. A minimum band of 20% was found to be an effective value.

V. Implementation In a Three Phase System

The system can be readily extended to a three-level three-phase system using three separate current regulators as follows. For each phase, the KVL load equation is:

$$V_x(t) = L\frac{dI_x(t)}{dt} + RI_x(t) + E_x(t) + U_0(t)\ ,\ x \in a,b,c \qquad (12)$$

where $U_0(t)$ is the load floating neutral point voltage.

The three-phase currents can be separated into non-interacting $I_x^s(t)$ and interacting $\gamma(t)$ components as [19][20]:

$$I_x(t) = I_x^s(t) + \gamma(t),\ x \in a,b,c \qquad (13)$$

The interacting current term part of (12) is now equated to the negative of the neutral point voltage $U_0(t)$, viz

$$L\frac{d\gamma(t)}{dt} + R\gamma(t) = -U_0(t) \qquad (14)$$

Eqn. (12) then can be simplified using (13) and (14), to give:

$$V_x(t) = L\frac{dI_x^s(t)}{dt} + RI_x^s(t) + E_x(t),\ x \in a,b,c \qquad (15)$$

With this reduction, (15) is identical to (1) for each individual phase current, which allows the previously developed single phase leg three-level variable hysteresis band concepts to be directly applied to the three phase system.

The interacting current can be calculated by recognising that the sums of the three phase currents and backemf voltages for a balanced three phase system are always zero. Hence summing (12) across all three phases results in:

$$U_0(t) = 1/3\left[V_a(t) + V_b(t) + V_c(t)\right] \qquad (16)$$

Since the resistive voltage drop $R\gamma(t)$ in (14) will always be small compared to the derivative term, the common mode interacting current can be adequately calculated using:

$$\gamma(t) = -\frac{1}{L}\int U_0(t)dt = \frac{1}{3L}\int\left[V_a(t) + V_b(t) + V_c(t)\right]dt \qquad (17)$$

It is then subtracted from the measured current before proceeding to the hysteresis comparison process.

VI. Experimental System

Fig. 9 shows how the new hysteresis current regulator was constructed for three phase three-level NPC and FC inverters with parameters as listed in Table II The load currents are measured by LEM LA-100P Hall Effect transducers. Op-amp summing junctions are then used to calculate the phase current errors and subtract the common mode interacting current. The resultant non-interacting errors feed into variable threshold analogue comparators whose outputs create the three-phase hysteresis switching signals $S_{a,tot}(t)$, $S_{b,tot}(t)$ $S_{c,tot}(t)$. The NPC and FC decoding logic and associated dead-time delay logic is then implemented in a MAX II CPLD, to create the inverter device output switching signals. The CPLD also generates the modified switching signals $S_{a,OR}(t)$, $S_{b,OR}(t)$, $S_{c,OR}(t)$ which feed into the timer/capture ports of the controlling DSP to trigger the average switching voltage calculation using (7). With this voltage, the DSP calculates the required variable hysteresis bands for each phase leg using (6) and (8), and outputs them through a DAC to create the variable hysteresis band threshold levels for the analog comparators.

The common mode interacting current is calculated using an additional DAC output from the DSP, scaled to match the measured positive bus voltage. This output (and its inverse) are processed through a multiplexer driven by the converter phase leg switching states, to create scaled representations of the phase leg three-level switched voltages. Next, these voltages are summed, integrated and scaled using op-amp analog circuitry as per (17), to create the common mode interacting current. Finally, this current is subtracted from the measured current to create the non-interacting current errors for the variable band hysteresis comparison.

VII. Single Phase Experimental Results

Fig. 10 shows the essentially constant switching frequency achieved by this scheme, with only a small residual frequency fluctuation. This is caused by a one switching cycle delay in the calculation of $V_{avg}(t)$ using (7), which introduces a slight error in the variable hysteresis band calculation (6).

Figs. 11(a)(b) show experimental results for the new controller operating with both fixed and variable hysteresis bands to regulate the current into a three-level NPC inverter. Fig. 11(c)(d) show experimental results with both fixed and

TABLE II: Multilevel Inverter Parameters.

Parameter		Value
Overall DC Link Voltage	($2*V_{DC}$)	200 V
Filter Inductance	(L)	18 mH
Output Resistance	(R)	0.5 Ω
Switching Frequency	(f_{sw})	2500 Hz
Fundamental Frequency	(f_o)	50Hz

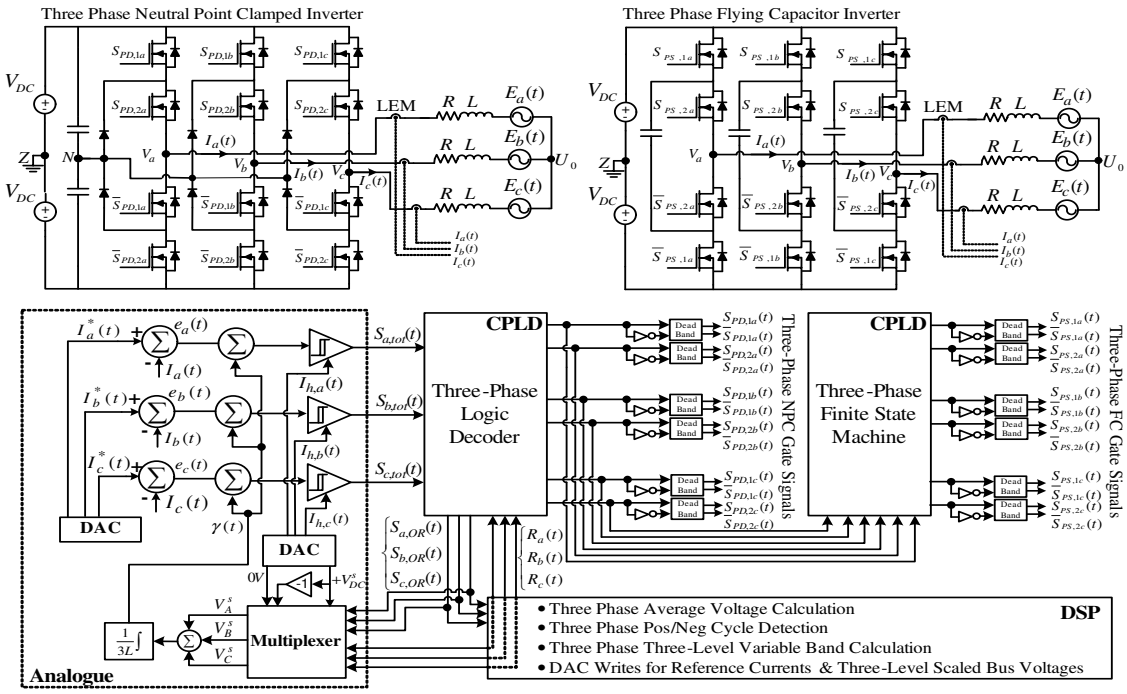

Fig. 9: Three phase three-level NPC inverter (left) and three phase three-level FC inverter (right) feeding backemf type load with three-level variable band hysteresis controller structure.

variable hysteresis bands to regulate the current into one phase of a three-level FC inverter. The figures show excellent output current tracking capability under both fixed and variable hysteresis band operation without any sign of DC tracking error. Also, it can be seen in these figures how the current error loops back from the hysteresis boundary without actually hitting it during the level change transition, while the controller smoothly continues switching after the polarity change. The figures also show a clear three-level switched phase voltage, especially at the zero voltage transition points. This confirms the effectiveness of the level selection strategy based on the prediction of the average voltage zero-crossing, which avoids the erroneous polarity transitions that are typical of normal multiband hysteresis implementations. Figs 11(c)(d) also show the balanced flying capacitor voltage, confirming the effectiveness of the active balancing strategy to maintain a balanced FC voltage using the FSM without requiring additional voltage measurement.

Fig. 12(left) shows the harmonic performance of the new hysteresis current regulator for the NPC inverter at a modulation depth of 0.9, illustrating how the use of a variable hysteresis band significantly improves the output voltage harmonic performance. For the NPC VSI, the WTHD is reduced from 1.64% for a fixed-band HCC to 1.32% for the variable band HCC with clock synchronisation. Fig. 12(right) shows the same level of harmonic improvement when the new hysteresis current regulator is applied to the FC inverter. By comparing these figures, it can be seen that the harmonic performance of the new hysteresis modulator is essentially identical irrespective of the three-level VSI topology. Both results also have a substantial direct carrier harmonic, similar to open PD PWM, which leads to substantial line-to-line harmonic cancellation for the three phase system since it is common mode to all three phases.

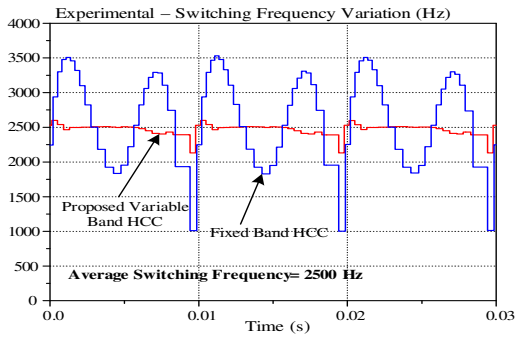

Fig. 10: Experimental switching frequency variation for fixed band and variable band hysteresis current control (Modulation Depth = 0.9)

VIII. Three Phase Experimental Results

Experimental results are respectively presented in Figs. 13 and 15 for the NPC inverter, and Figs 14 and 16 for the FC inverter, for a pulse ratio of 50 ($f_s = 2500Hz, f_o = 50Hz$). Fig. 15(a) and Fig. 16(a) show the distinctive pattern of PD modulation in the five-level line-to-line voltages (switching always constrained between two successive voltage levels at any point in time), although with some leakage because of hysteresis band clamping during voltage level transitions, as shown in Fig 8. Figs. 15(b) and 16(b) confirm this result, showing harmonic line voltage spectra with no common mode carrier harmonic in the line-line voltage as anticipated from the single phase results.

Fig 17(a)(b) shows the system's transient response achieved for a 100% step-up change in reference current for the NPC and FC inverters, which confirms that the variable hysteresis band addition has not compromised the excellent

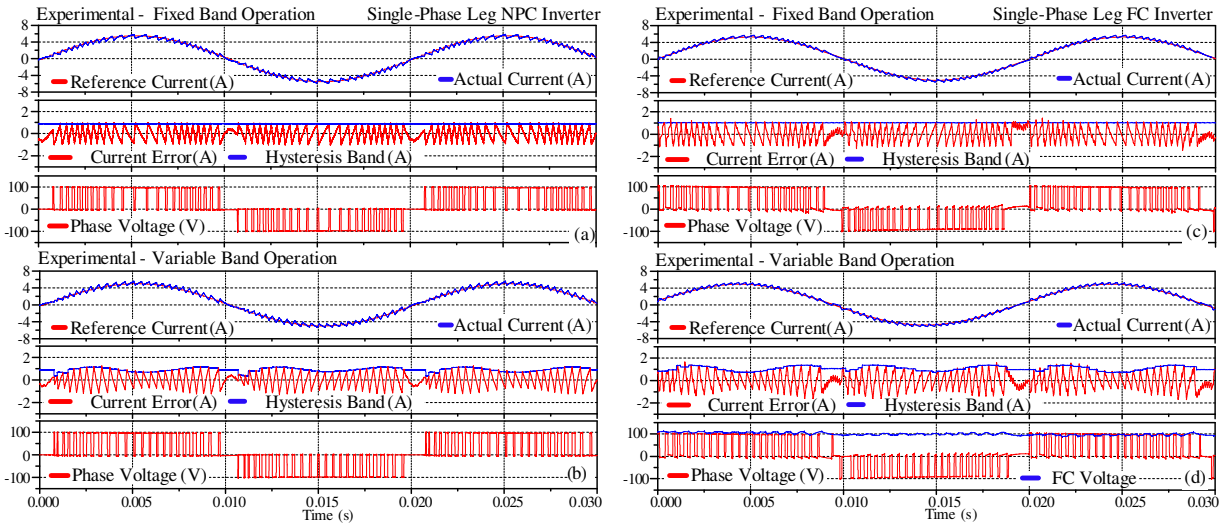

Fig. 11: Experimental results of the proposed three-level hysteresis controller ((top) Output current, (middle) Current error & hysteresis band, (bottom) Phase Voltage) (a) Fixed band operation/NPC inverter (b) Variable band operation/NPC inverter (c) Fixed band operation/FC inverter (d) Variable band operation/FC inverter

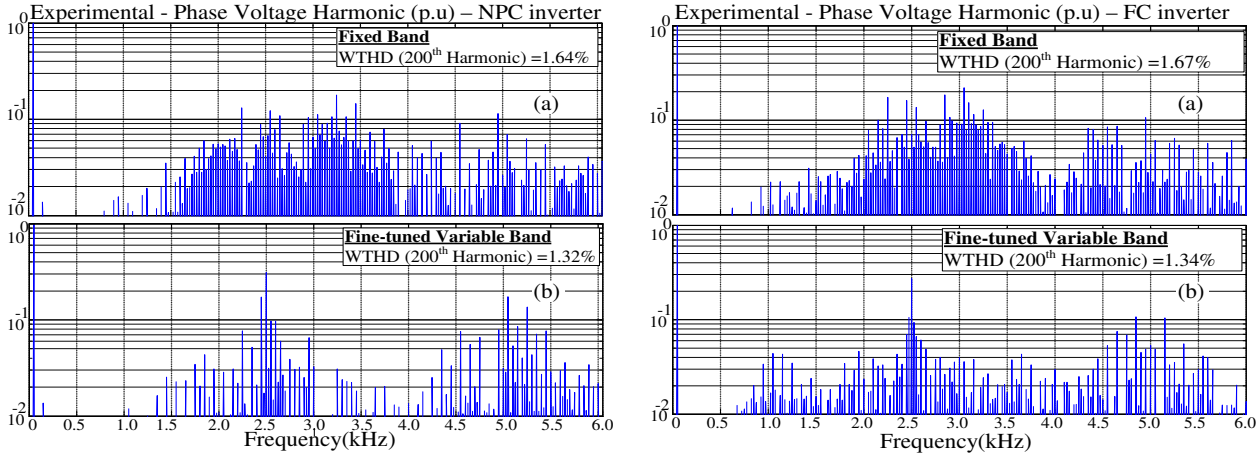

Fig. 12: Experimental phase leg voltage harmonics of single phase leg (left) NPC inverter (right) FC inverter under hysteresis current regulation. (a) fixed band (b) variable band with clock synchronization ($f_{sw}/f_o=50$, modulation depth = 0.9)

dynamic response of the conventional hysteresis control [6]. Note also how the variable band fluctuation increases after the transient due to the resultant increase in load back-emf.

IX. Conclusion

This paper has presented a new variable band hysteresis regulation strategy for a three level NPC and FC multilevel inverter. The strategy uses the averaged voltages of the phase leg switched outputs to vary the hysteresis bands so as to maintain a near constant phase leg switching frequency. The same average output voltages are then used to detect the polarity change of each phase leg voltage, allowing their phase leg switchings to be controlled using a single hysteresis comparator (in conjuction with some simple combination logic). These improvements significantly improve the performance of the system compared to previous multilevel hysteresis approaches. Finally, the common mode interacting current for a three phase system is removed before hysteresis control of each phase leg, to achieve high quality, high performance current regulation with a harmonic performance that is very close to open loop PD PWM.

X. References

[1] A. Nabae; I. Takahashi, H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," IEEE Trans. on, Ind. Appl., vol.IA-17, no.5, pp.518-523, Sept. 1981.

[2] J. Rodriguez, et al., "Multilevel inverters: a survey of topologies, controls, and applications," Industrial Electronics, IEEE Transactions on, vol. 49, pp. 724-738, 2002.

[3] D. Krug, et al., "Comparison of 2.3-kV Medium-Voltage Multilevel Converters for Industrial Medium-Voltage Drives," Industrial Electronics, IEEE Transactions on, vol. 54, pp. 2979-2992, 2007.

[4] J. Rodriguez, L.G. Franquelo, S. Kouro, J.I. Leon, R.C. Portillo, M.A.M. Prats, M.A. Perez, "Multilevel Converters: An Enabling Technology for High-Power Applications" *Proceedings of the IEEE*, vol.97, no.11, pp.1786-1817, Nov. 2009.

[5] J. Holtz, "Pulsewidth modulation-a survey, "*Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*, vol., no., pp.11-18 vol.1, 29 Jun-3 Jul 1992.

[6] M.P. Kazmierkowski, L. Malesani, "Current control techniques for three-phase voltage-source PWM converters: a survey" IEEE Trans. on, Ind. Electron., vol.45, no.5, pp.691-703, Oct 1998.

[7] M. A. Rahman, T. S. Radwan, A. M. Osheiba, and A. E. Lashine, "Analysis of current controllers for voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 44, No. 4, pp. 477-485, Aug. 1997.

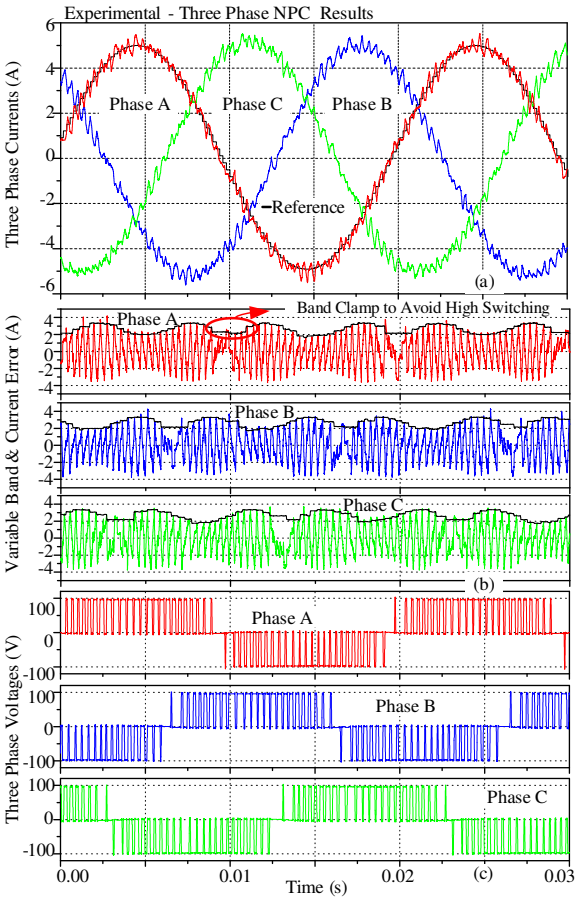

Fig. 13: Experimental results of the proposed controller for three-level NPC inverter (f_{sw}/f_o=50, *modulation depth=0.9*). Three phase (a) output currents (b) current errors and variable bands (c) phase voltages

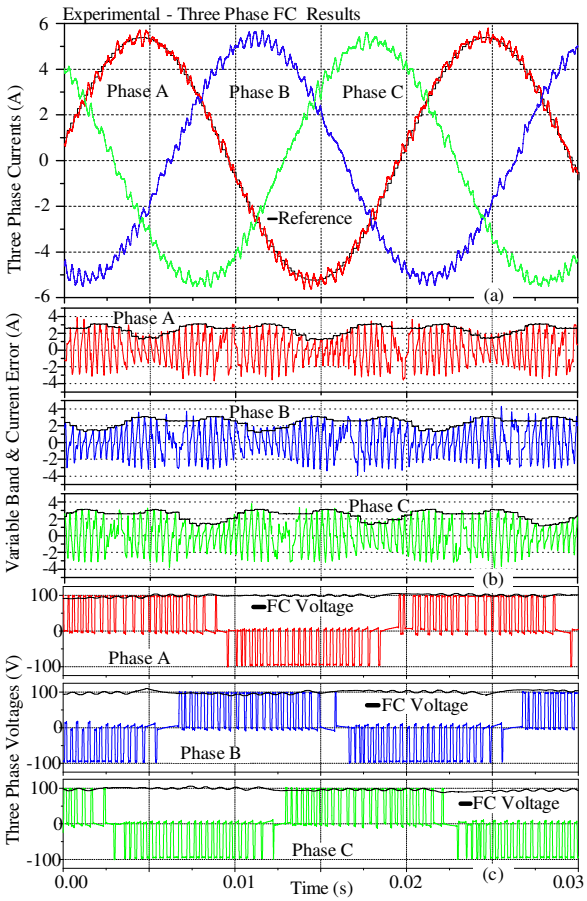

Fig. 14: Experimental results of the proposed controller for three-level FC inverter (f_{sw}/f_o=50, *modulation depth=0.9*). Three phase (a) output currents (b) current errors and variable bands (c) phase voltages

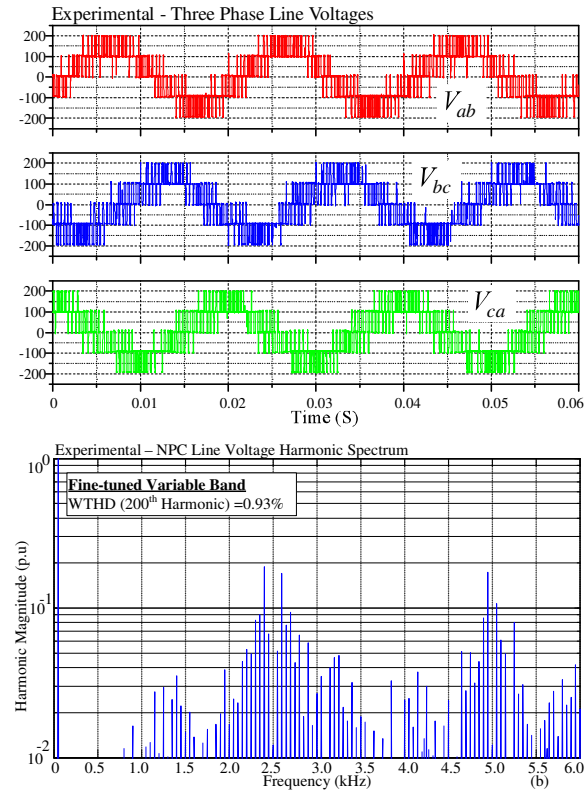

Fig. 15: Experimental results of three phase NPC (a) line voltages (b) Line to line harmonic spectrum, (f_{sw}/f_o=50, *modulation depth=0.9*).

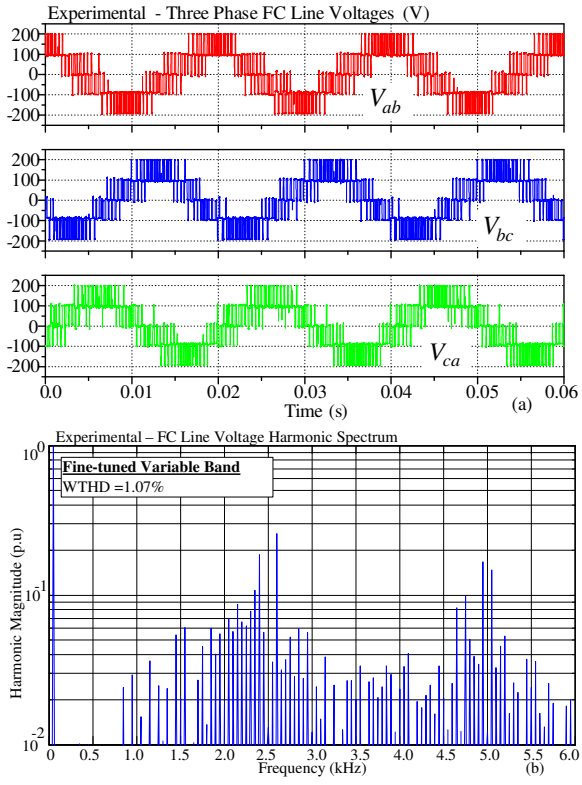

Fig. 16: Experimental results of three phase FC (a) line voltages (b) Line to line harmonic spectrum, (f_{sw}/f_o=50, *modulation depth=0.9*).

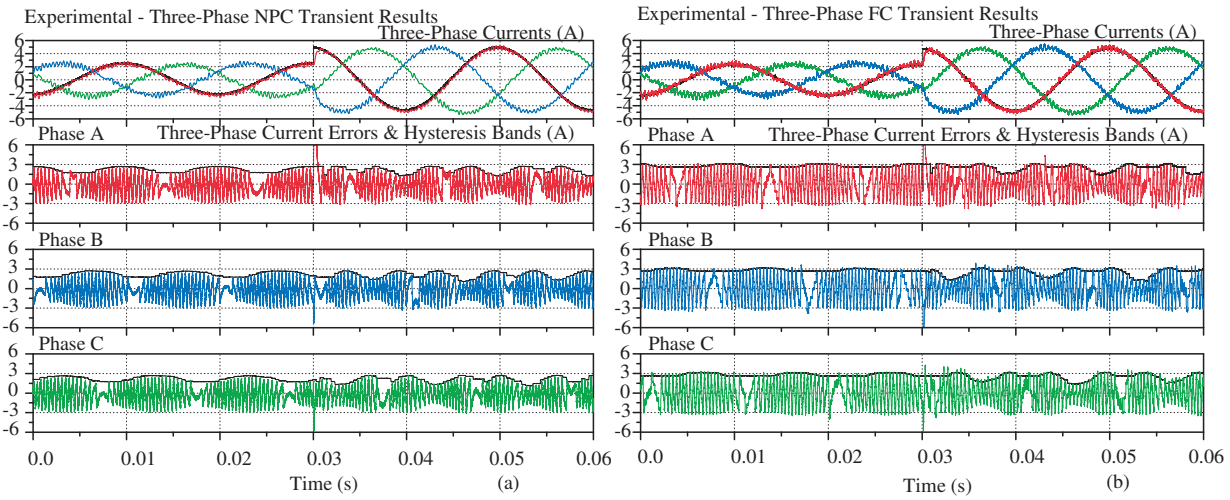

Fig. 17: Experimental transient operation of the proposed three-level hysteresis current regulator showing output currents, current errors and variable hysteresis bands - 100% commanded step change in current (a) NPC inverter (b) FC inverter

[8] S. Buso, S. Fasolo, L. Malesani and P. Mattavelli, "A Dead-Beat Adaptive Hysteresis Current Control," *IEEE Transactions on Industry Applications,* Vol. 36 No. 4, July/Aug 2000, pp. 1174-1180.

[9] L. Malesani, P. Tenti, "A novel hysteresis control method for current-controlled voltage-source PWM inverters with constant modulation frequency," *IEEE Trans. Ind. Appl.*, vol.26, no.1, pp.88-92, Jan 1990.

[10] A. Shukla, A. Ghosh, A. Joshi, "Hysteresis Modulation of Multilevel Inverters" IEEE Trans. on , Power Electron., vol.26, no.5, pp.1396-1409, May 2011.

[11] M. Marchesoni, "High performance current control techniques for applications to multilevel high-power voltage source inverters," *IEEE Trans. Power Electron.*, pp. 189–204, vol. 7, no. 1, Jan. 1992.

[12] R. Gupta; A. Ghosh, A. Joshi, A, "Multiband Hysteresis Modulation and Switching Characterization for Sliding-Mode-Controlled Cascaded Multilevel Inverter," Industrial Electronics, IEEE Transactions on , vol.57, no.7, pp.2344-2353, July 2010

[13] F. Zare; G. Ledwich, "A hysteresis current control for single-phase multilevel voltage source inverters: PLD implementation," Power Electronics, IEEE Trans. on, vol.17, no.5, pp. 731- 738, Sep 2002.

[14] P. C. Loh, G. H. Bode, D.G.Holmes, and T.A. Lipo, "A time-based double band hysteresis current regulation strategy for single phase multilevel inverters," *IEEE Trans. Ind. Appl.*, vol. 39, no. 3, pp. 883–892, May/Jun. 2003.

[15] Huifeng Mao, et al, "A Hysteresis Current Controller for Single-Phase Three-Level Voltage Source Inverters," Power Electronics, IEEE Transactions on , vol.27, no.7, pp.3330,3339, July 2012.

[16] K. Gopakumar, et al., "A Space Vector based Hysteresis Current Controller for a General n-level Inverter Fed Drive with Nearly Constant Switching Frequency Control," Industrial Electronics, IEEE Transactions on , vol.PP, no.99, pp.1, 0, Mar. 2012.

[17] R. Ramchand, et al., "Improved switching frequency variation control of hysteresis controlled voltage source inverter-fed IM drives using current error space vector," Power Electronics, IET, vol.3, no.2, pp.219-231, Mar 2010.

[18] T. Ghennam, E.M. Berkouk, B. Francois, "A Novel Space-Vector Current Control Based on Circular Hysteresis Areas of a Three-Phase Neutral-Point-Clamped Inverter," Industrial Electronics, IEEE Transactions on , vol.57, no.8, pp.2669-2678, Aug. 2010.

[19] R. Davoodnezhad, D.G Holmes, B.P McGrath, " Constant frequency three phase hysteresis current regulator with extended modulation depth," Power Electronics and Motion Control Conference (IPEMC), 2012 7th International, vol.1, no., pp.263-268, 2-5 June 2012.

[20] Holmes, D.G.; Davoodnezhad, R.; McGrath, B.P.; "An Improved Three-Phase Variable-Band Hysteresis Current Regulator," Power Electronics, IEEE Transactions on, vol.28, no.1, pp.441-450, Jan. 2013.

[21] B. P. McGrath, et al., "Optimal Modulation of Flying Capacitor and Stacked Multicell Converters Using a State Machine Decoder," Power Electronics, IEEE Transactions on, vol. 22, pp. 508-516, 2007.