Single-Phase Semi-Bridge Five-Level Flying-Capacitor Rectifier

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***Abstract*—For unity power factor applications such as grid-connected rectifiers, semi-bridge converters offer significant advantages over their full-bridge counterparts because of their reduced active switch count and shoot-through-free phase leg structure. However, semi-bridge rectifiers have intrinsic operating limits that require a tradeoff between current distortion and switching ripple. This paper presents a new single-phase semi-bridge flying-capacitor (FC) rectifier that significantly improves this tradeoff, with effective doubling in switching frequency because of the multilevel topology, and the capability to rectify higher output voltages with lower voltage rated, more efficient, devices. For rectifier applications, the new topology offers a better balance between cost and performance than either a diode rectifier followed by a single-phase-leg three-level boost power factor corrector (PFC) or a full-bridge single-phase five-level FC rectifier. Matching simulation and experimental results are presented to fully validate the new converter structure.**

***Index Terms*—AC–DC power converters, flying-capacitor converters, multilevel converters, rectifiers, semi-bridge converters.**

I. Introduction

PRESENT-DAY standards and market needs for electronic equipment increasingly require active single-phase rectifiers that can operate over a wide supply voltage range with low input current distortion and ripple, near-unity power factor, and high efficiency and power density. For unity power factor rectifiers that do not require a bidirectional power flow capability, the boost power factor corrector (PFC) rectifier is a common solution. This topology consists of a single semi-bridge phase leg enclosed within a full-bridge diode rectifier, controlled as a conventional step-up dc–dc converter to boost the rectified ac input voltage to a higher voltage dc bus. However, the arrangement has the disadvantage of three series device voltage drops in the incoming conduction path, which limits its maximum possible efficiency [1]. An alternative topology is a fully controlled single-phase H-bridge, which has only two series device voltage drops but has the substantial expense of requiring four active switched devices. For unity power factor active rectifiers, the attractive reduction of this arrangement is to then replace the active switch in each upper phase leg with a simple diode to create the single-phase semi-bridge topology [2]–[5].

For higher power and higher voltage applications, it is well recognized that multilevel converters can offer benefits of reduced semiconductor voltage ratings for a given dc bus voltage and superior harmonic performance for a given switching frequency because of the harmonic cancelation that can be achieved [6], [7]. These benefits allow a better tradeoff between efficiency, switching frequency, and filter inductance than their two-level counterparts. Of the three major multilevel converter topologies that have become established over recent years, the flying capacitor (FC) has the particular benefits of a modular structure and no requirement for individual isolated dc sources [8]. These advantages are of primary interest for rectifier applications.

This paper presents a new multilevel semi-bridge rectifier structure based on the FC topology that capitalizes on these advantages. The structure offers the twin benefits of reduced semiconductor voltage stress for a given dc output voltage, allowing lower voltage rating devices with reduced conduction losses to be used, and cancelation of the first carrier group switching harmonics, allowing a much smaller input filter inductor to be used. This second benefit also significantly improves the zero-crossing distortion of the rectifier compared with its two-level counterpart by allowing a reduced-per-unit boost filter inductance to be used [4]. The work is verified by detailed simulation and matching experimental results.

II. Single-Phase Semi-Bridge FC Rectifier

Fig. 1(a) shows a previously reported boost PFC rectifier that uses a topologically reduced three-level FC phase leg to control the dc–dc voltage boost process [9]. The use of the reduced FC phase leg allows operation at higher dc output voltages compared with the standard single-switch PFC structure. However, the input rectifier diodes are still rated at the full dc output voltage, and hence, their forward voltage drop will be higher than for lower voltage-rated devices. This limits the maximum rectifier efficiency.

Fig. 1(b) shows a single-phase five-level full-bridge rectifier constructed from two individual FC phase legs. When controlled by pulsewidth modulation (PWM) with the correct phase displacement of fundamental voltage references and carriers [10], this converter offers improved harmonic cancelation and stronger natural balancing of the FC voltages compared with the boost PFC rectifier shown in Fig. 1(a). However, the number of active switches is a significant disadvantage of this approach.

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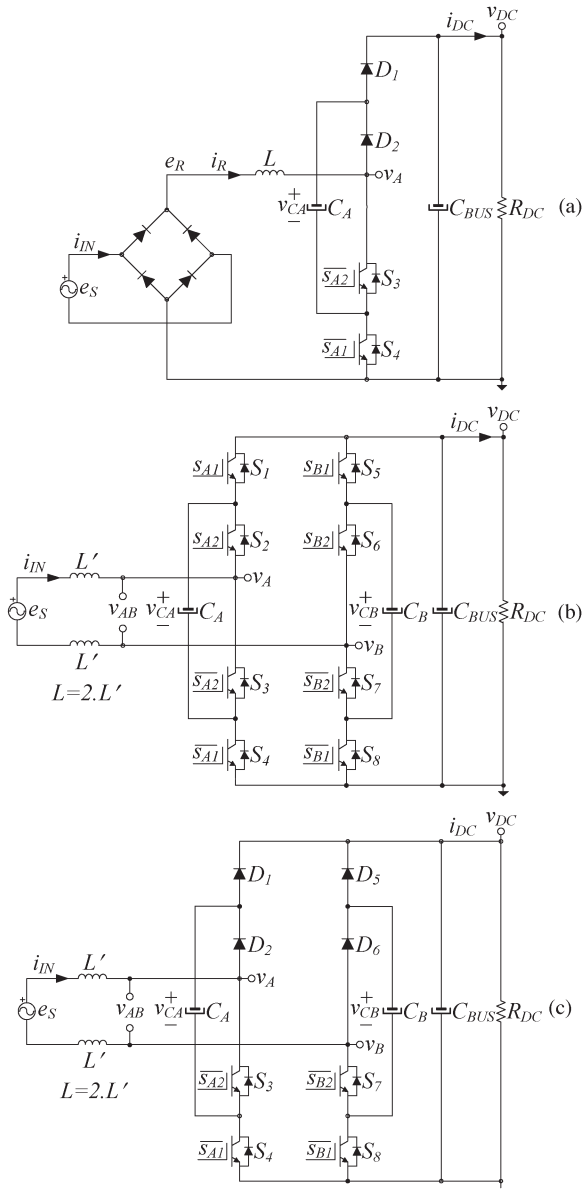

Fig. 1. Single-phase FC rectifiers: (a) boost PFC [9], (b) conventional full-bridge FC rectifier, and (c) new semi-bridge FC rectifier.

Fig. 1(c) shows the new reduced topology semi-bridge FC rectifier presented in this paper, where the two active upper switches in each phase leg have been replaced by simple diodes. This arrangement minimizes the system active switch count, allows the use of more efficient lower voltage-rated devices, and also avoids deadtime distortion in the switching processes between the active switches.

All semi-bridge and boost PFC rectifiers are well known to produce a low-frequency input current distortion cusp when operating in continuous conduction mode (CCM) because of their inherent inability to operate in the second and fourth quadrants, as identified in Fig. 2. Since this distortion increases with a larger boost filter inductance, semi-bridge rectifier design is a balance between reducing the low-frequency current distortion with a smaller size of filter inductance, at the expense of increased ripple current, and increasing the filter inductance size to reduce ripple current, at the expense of increasing the low-frequency current distortion, as discussed in [4]. This tradeoff is more challenging for low pulse ratio applications such as airborne rectifiers with supply frequency ranging from 360 to 800 Hz [11], or higher power applications where the lower switching frequency may require a larger value filter inductance to achieve an acceptable level of switching current ripple.

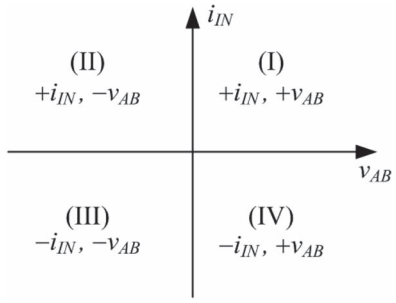

Fig. 2. Quadrants of operation of a full-bridge converter.

This new semi-bridge FC converter significantly assists this tradeoff since the input inductor size can be reduced by up to a factor of four for the same operating conditions because the effective input current switching frequency is twice the operating switching frequency. In addition, since the main sources of loss for an active rectifier are the switching processes and device forward voltage drops, a reduced operating switching frequency and the use of lower voltage-rated semiconductor devices can achieve improved overall efficiency despite the higher number of devices in the forward conduction path [9].

III. Operating Modes and Intrinsic Limitation

The single-phase full-bridge five-level FC converter shown in Fig. 1(b) has 16 operating states [12], which allow its switched voltage v_{AB} to assume one of the five voltage levels $(-v_{\rm DC}, -v_{\rm DC}/2, 0\ {\rm V}, +v_{\rm DC}/2, +v_{\rm DC})$ irrespective of the direction of grid input current $i_{\rm IN}$. It is this flexibility of operation that gives a full-bridge rectifier the capability to operate in all four quadrants shown in Fig. 2 because it can produce a switched output voltage of either polarity for both positive and negative input currents.

In contrast, the single-phase semi-bridge five-level FC rectifier in Fig. 1(c) has only the eight possible conduction states shown in Fig. 3 because of the lack of a reverse-polarity current path through the upper phase leg switches. Hence, when $i_{\rm IN}$ is positive, only phase leg A can switch between its various voltage states, whereas the return current through phase leg B must always flow through the antiparallel diodes of switches S_7 and S_8. Similarly, when $i_{\rm IN}$ is negative, only phase leg B can switch between its voltage states, and the return current through phase leg A must always flow through the antiparallel diodes of switches S_3 and S_4. Consequently, the converter can only operate in quadrants I and III, where converter switched voltage v_{AB} and input current $i_{\rm IN}$ have the same polarity.

For operation as an active rectifier at unity power factor and continuous conduction (the usual mode for higher power rectifiers), the commanded fundamental voltage reference is slightly displaced from the incoming ac grid voltage to regulate the power flow through the input boost filter to maintain a stable voltage on the dc output bus. Fig. 4 shows an averaged

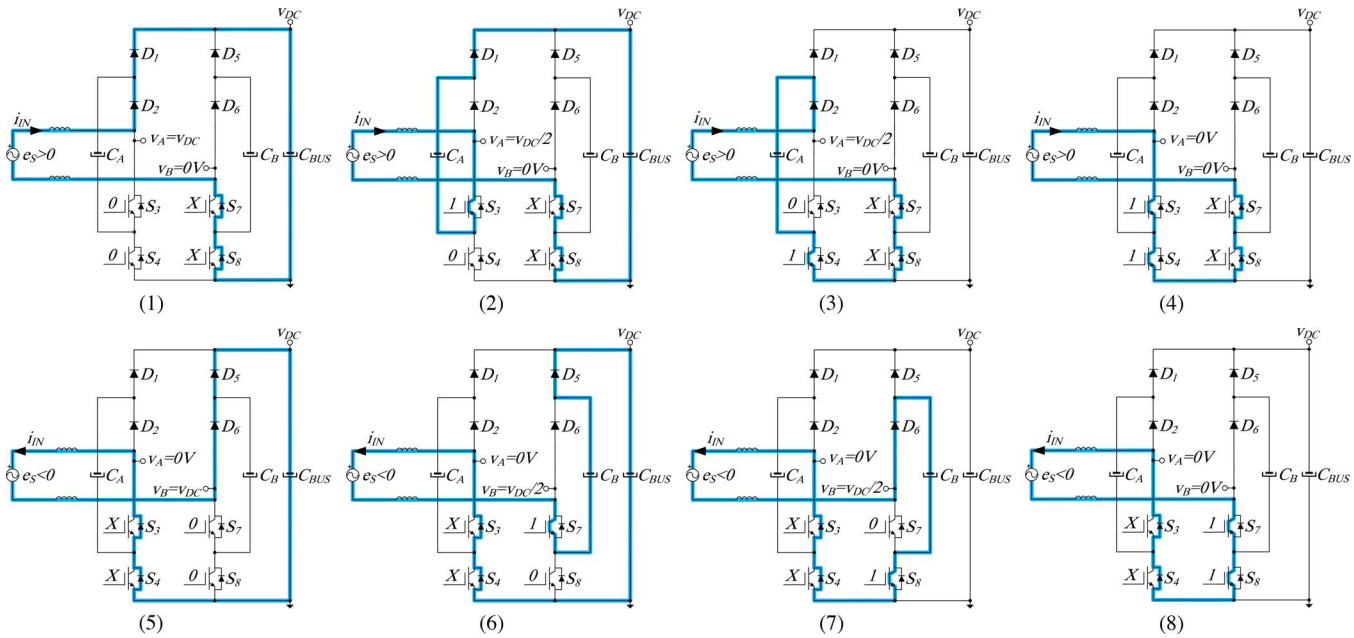

Fig. 3. Operating modes of a single-phase semi-bridge five-level FC rectifier when working in CCM at unity power factor.

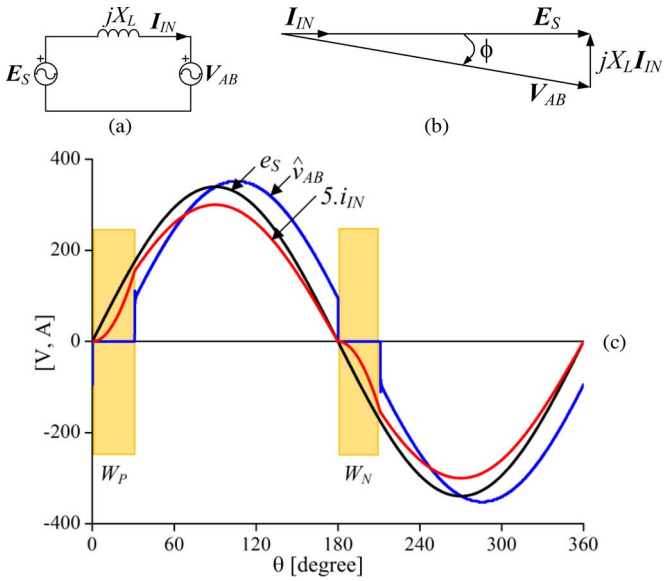

Fig. 4. Single-phase semi-bridge FC rectifier operating in CCM: (a) averaged representation, (b) phasor diagram for unity power factor, and (c) supply voltage, input current, and averaged switched rectifier voltage.

representation of this condition, with the average of the converter switched voltage represented as phasor V_{AB}. This figure illustrates the intrinsic operating limitation of a semi-bridge rectifier and the resulting cusp distortion in the input current. Since switched rectifier voltage v_{AB} must always have the same polarity as input current $i_{\rm IN}$, current regulation is not possible when the input current goes through zero since an opposite-polarity commanded converter voltage is required during this region to maintain proper current control. Hence, the converter switched voltage clamps to zero, and the input current freewheels through the cusp distortion locus shown in Fig. 4 until it intersects the commanded sinusoidal input current some time later. Once this occurs, converter modulation recommences and current control is re-established.

The phase displacement between commanded fundamental voltage reference $\hat{v}_{AB}$ and incoming ac grid voltage e_S depends on the active power transferred to the load, the magnitude of the input filter inductance (including the grid impedance), and a number of second-order effects, as analyzed in detail in [4]. In principle, minimum distortion is achieved with the smallest possible input filter inductance, provided that the switching ripple in the ac current is acceptably small to meet required harmonic standards. With a multilevel converter, the same switching ripple current magnitude can be achieved with a smaller filter inductance because of the higher effective output switching frequency of the overall converter.

IV. Optimum FC Semi-Bridge Modulation

For the full-bridge single-phase FC converter shown in Fig. 1(b), optimum harmonic cancelation is achieved when two 180° displaced fundamental reference signals m_A and m_B are used for each of the phase legs, with the four complementary sets of switches modulated by carriers that are phase shifted by 90°, as shown in Fig. 5, for a modulation depth $M = 0.9$ and pulse ratio $f_C/f_O = 5$ [12]. This strategy cancels the first carrier group harmonics within each switched phase leg output voltage and then cancels the second carrier group harmonics across line-to-line switched output voltage v_{AB}. It also provides a strong natural balancing force to maintain intermediate capacitor voltages v_{CA} and v_{CB} at exactly $v_{\rm DC}/2$. Note also the five-level switched output voltage created by this strategy.

Since only one phase leg of the single-phase semi-bridge five-level FC converter can be switched at any one time, it must be controlled using 180° discontinuous modulation [13]. Hence, there is no benefit in phase-shifting carriers between the two phase legs. Optimum harmonic cancelation is therefore achieved with the simpler carrier phase shift of only 180° for each phase leg, as shown in Fig. 6 (now for a pulse ratio $f_C/f_O = 10$, twice as for the full-bridge, to maintain the same

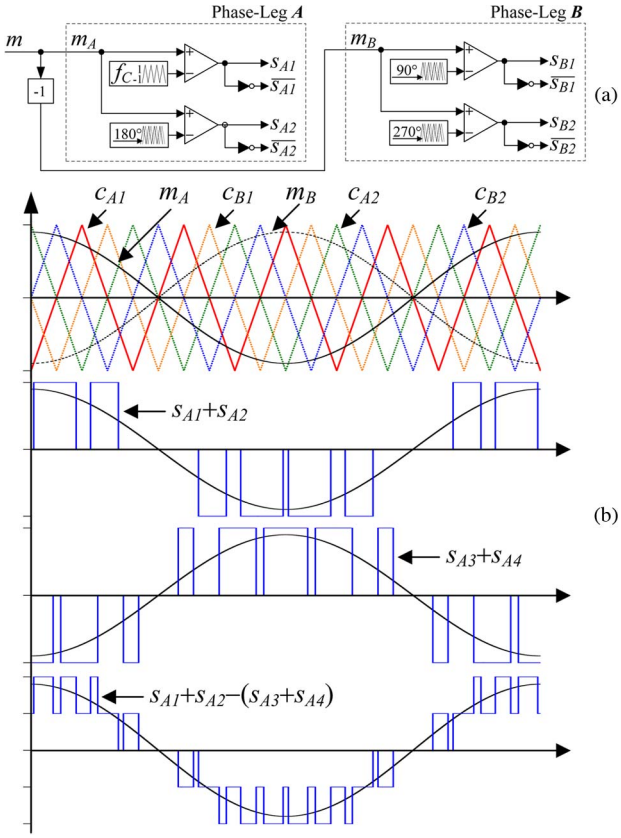

Fig. 5. Naturally sampled modulation of a single-phase five-level full-bridge FC converter: (a) structure and (b) waveforms (open-loop, M = 0.9, f_C/f_O = 5).

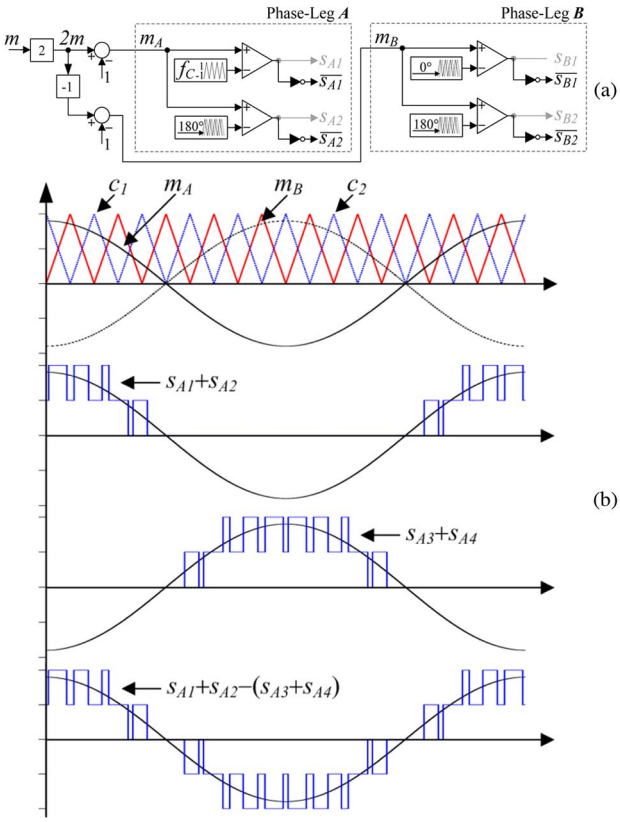

Fig. 6. Naturally sampled modulation of a single-phase five-level semi-bridge FC converter: (a) structure and (b) waveforms (open-loop, M = 0.9, f_C/f_O = 10).

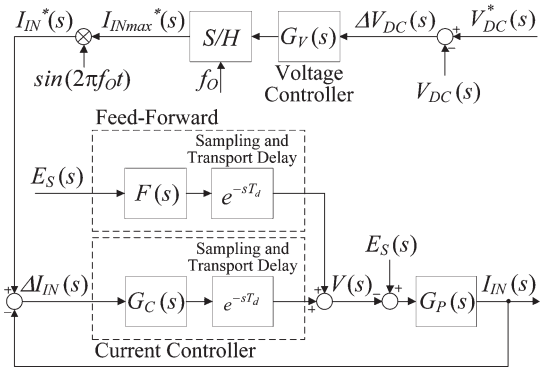

Fig. 7. Cascaded outer dc bus voltage inner input current control system.

overall number of switching transitions). Of course, this means that only the first carrier group harmonics will be canceled in line-to-line output voltage v_{AB}, but this is an unavoidable consequence of semi-bridge operating limitations.

Note that despite the discontinuous and rather different phase leg switched waveforms of the semi-bridge phase legs, the topology still achieves the same five-level output voltage switching pattern of a full-bridge, and hence, the natural balancing force acting on capacitor voltages v_{CA} and v_{CB} remains as strong as for the full-bridge case.

V. Cascaded Control System

A similar cascaded control scheme as was used for a two-level semi-bridge rectifier [4] is now applied to this multilevel converter to manage the rectification process. As shown in Fig. 7, the controller comprises an outer dc bus voltage PI control loop, which generates a commanded current reference that feeds into an inner-loop PI current regulator.

From Fig. 7, $V_{\rm DC}(s)$ is the commanded dc bus voltage; $I_{\rm IN}(s)$ is the required input current, which is calculated by multiplying the current magnitude commanded by the dc voltage loop with a sinusoid that is synchronized to the grid; $V(s)$ is the average commanded voltage fed to the PWM modulator from the current regulator; and $E_S(s)$ represents the grid back electromotive force (EMF). The voltage difference $E_S(s) - V(s)$ feeds through the plant representation $G_P(s)$ to produce the actual grid current $I_{\rm IN}(s)$. In addition, as shown in Fig. 7, feedforward compensation of the grid back EMF voltage has been added to the controller to reduce the steady-state ac current error [14]. Note as well that the $V_{\rm DC}$ gain provided by the PWM modulator has been integrated into the controller block function $G_C(s)$ for simplicity.

The plant transfer function is given by

$$G_P(s) = \frac{1}{R}\left(\frac{1}{1+sT_P}\right) \tag{1}$$

where $T_P = L/R$, with R representing the filter resistance and L including both the filter and grid inductances. The current regulator uses a simple PI controller given by

$$G_C(s) = k_{PI}V_{\rm DC}\left(1+\frac{1}{s\tau_{II}}\right). \tag{2}$$

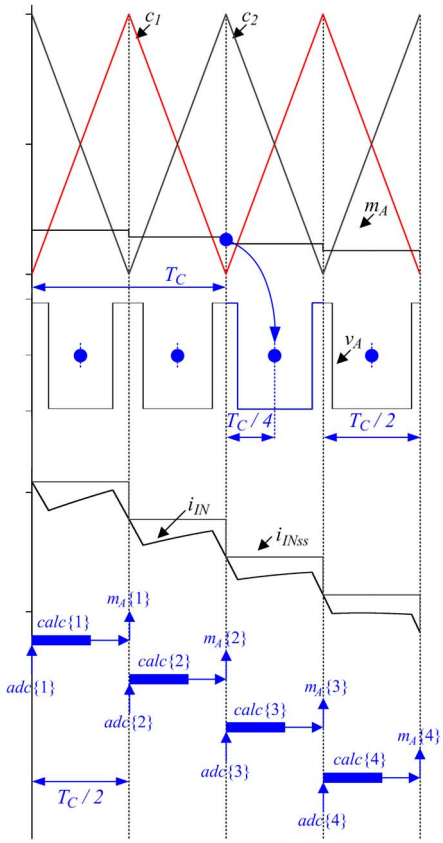

Fig. 8. Computation and transport delays caused by the PWM process and digital controller sampling/computation.

For this controller, k_{PI} is the proportional gain, and τ_{II} is the integrator gain (expressed as a time constant).

The optimized determination of these gains must take into account both the inherent quarter-carrier-period transport delay of asymmetrical regular sampled PWM and the half-carrier computation delay caused by the synchronously sampled current measurement adopted to filter the switching ripple current, as shown in Fig. 8. From this figure, it is shown how the modulation command m_A for phase leg A is frozen at the start of each half-carrier period $T_C/2$ and compared against triangular carriers c_1 and c_2 to create the switch operating states as the carriers cross this sampled command signal. Intrinsically, this process introduces a $1/4T_C$ transport delay into the control loop. In addition, the grid current i_{IN} is acquired at every half-carrier period to become the synchronously sampled input current i_{INss}. Since the process of analog-to-digital conversion and calculation takes a finite amount of time, a new value for the modulation command m_A is therefore only available after a $1/2T_C$ delay. Using the design principles described in [14] and adopting a phase margin of 50°, the optimal values for k_{PI} and τ_{II} were calculated using these concepts to be 0.23 A^{-1} and 2.15 ms, respectively, for the system parameters defined in Table I.

The dc bus voltage regulator also uses a simple PI controller, given by

$$G_V(s) = k_{PV}\left(1 + \frac{1}{s\tau_{IV}}\right) \tag{3}$$

TABLE I
EXPERIMENTAL SYSTEM PARAMETERS

Description	Label	Value
Supply voltage	e_S	240 [V_{rms}]
Supply frequency	f_O	50 [Hz]
Input power	P	950 [W]
Filter + grid inductances (L_{pu} = 0.097)	L	18.8 [mH]
Bus Capacitance	C_{BUS}	4290 [μF]
Flying-caps capacitance	C_A, C_B	110 [μF]
Switching frequency	f_C	5 [kHz]
Load resistance	R_{DC}	170 [Ω]
Balance booster	R_{BB}	100 [Ω]
	L_{BB}	1.5 [mH]
	C_{BB}	690 [nF]
Target DC bus voltage	V^*_{DC}	380 [V]
Input current controller gains		
Proportional	k_{PI}	0.23 [A^{-1}]
Integral	τ_{II}	2.15 [ms]
DC bus voltage controller gains		
Proportional	k_{PV}	0.05 [AV^{-1}]
Integral	τ_{IV}	200 [ms]

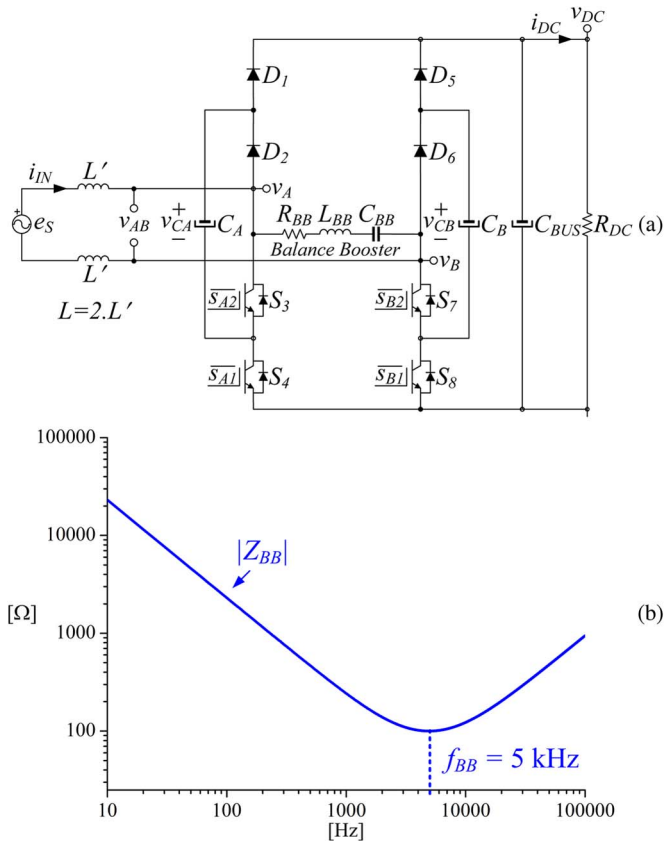

Fig. 9. Balance booster: (a) circuit arrangement and (b) magnitude of the balance booster impedance Z_{BB} as a function of frequency for the experimental system parameters.

where k_{PV} is the proportional gain, and τ_{IV} is the reciprocal of the integrator gain. These two gains were empirically adjusted, resulting in values of 0.05 AV^{-1} and 200 ms, respectively, as listed in Table I, to achieve an acceptable performance.

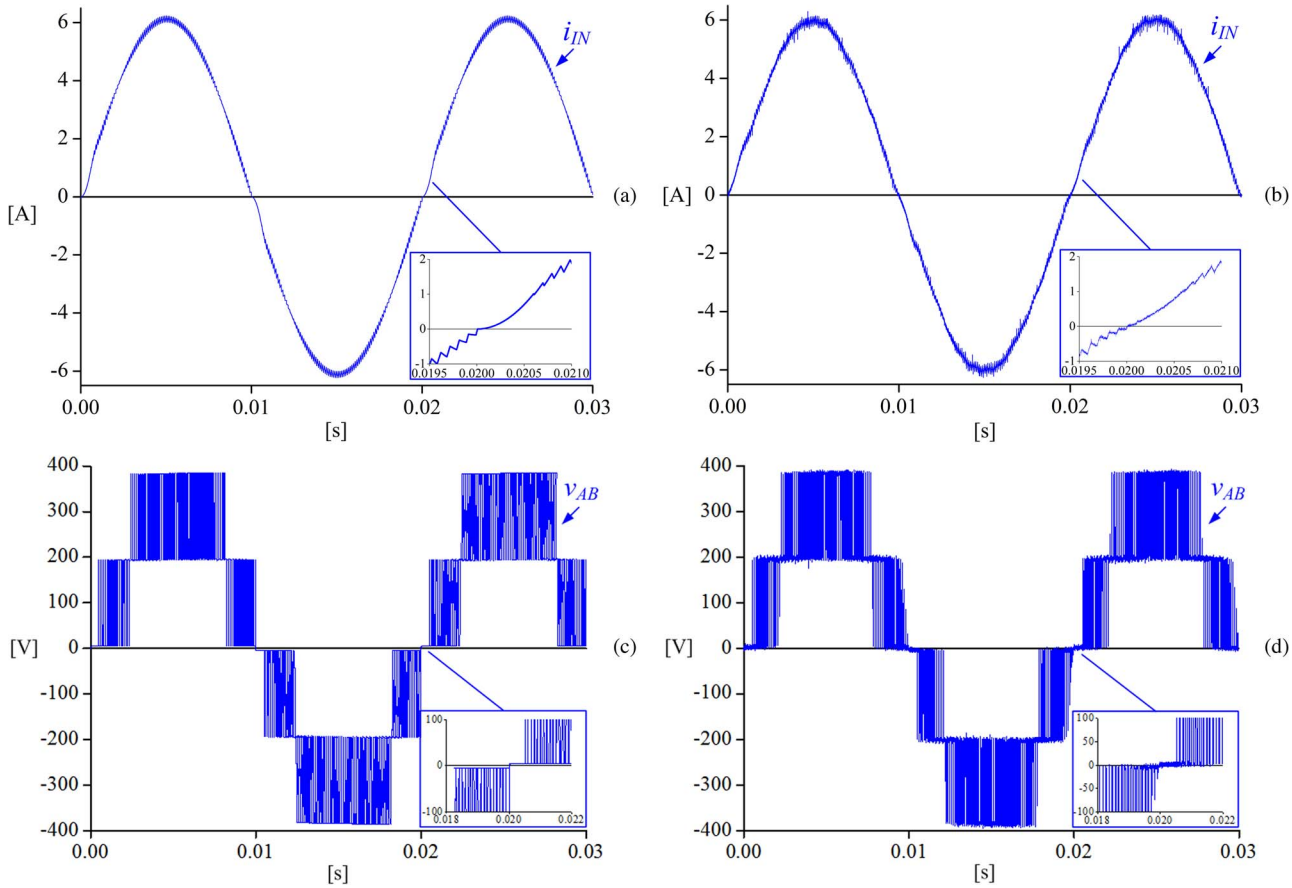

Fig. 10. (Left) Simulation and (right) experimental results: (a) and (b) input current and (c) and (d) rectifier switched output voltage.

The use of feedforward compensation of the grid voltage minimizes the burden of the current controller, allowing a smaller integral action to be used [14]. This is particularly advantageous for a semi-bridge converter since this topology has a potential for integral windup during the uncontrollable cusp intervals, which could result in current overshoot when leaving these regions. However, as shown in Fig. 10(a) and (b), no identifiable overshoot occurs using the proposed control methodology.

VI. FC Voltage Balance

One of the benefits of phase-shifted carrier (PSC)-PWM is the relatively strong natural voltage balancing forces created by this modulation scheme. However, since previous work has shown that this balancing force is proportional to the level of current ripple [10], the benefit of the semi-bridge FC converter in reducing the current ripple directly works against the natural balancing force. Two solutions are possible to resolve this conflict, i.e., either use active closed-loop control to measure the capacitor voltage unbalance and adjust each phase leg modulation accordingly [9] or include a passive series $R_{\rm BB}L_{\rm BB}C_{\rm BB}$ balance-boost notch filter between the phase legs [15]–[17] and tune this filter to the first carrier group harmonics, as shown in Fig. 9. This simpler second strategy was used for the work described in this paper.

The balance booster mechanism is readily understood using a frequency-domain perspective, as follows. Any unbalance in FC voltages v_{CA} and v_{CB} produces first carrier group voltage harmonics in phase leg switched voltages v_A and v_B, as identified in [18]. The balance booster path in Fig. 9(b) has low impedance at this carrier frequency, providing a path for the flow of current harmonics from this carrier group. The current flow continues until no first carrier group voltage harmonics remain in phase leg switched voltages v_A and v_B (this situation is the signature of a balanced voltage condition for an FC converter).

In principle, the balance booster action is voltage driven and does not directly depend on load current. However, damping resistor $R_{\rm BB}$ incurs losses because second carrier group current harmonics continue to flow through the balance booster, even when the FC cell voltage is balanced. Reference [18] presents an analysis strategy to balance the cell voltage settling time constant against resistive losses.

VII. Simulation and Practical Validation

The operation of proposed topology has been extensively investigated in both simulation and matching experimental investigations for an experimental FC system with the parameters described in Table I. The control systems were implemented on a TI fixed-point TMS320F2810 DSP.

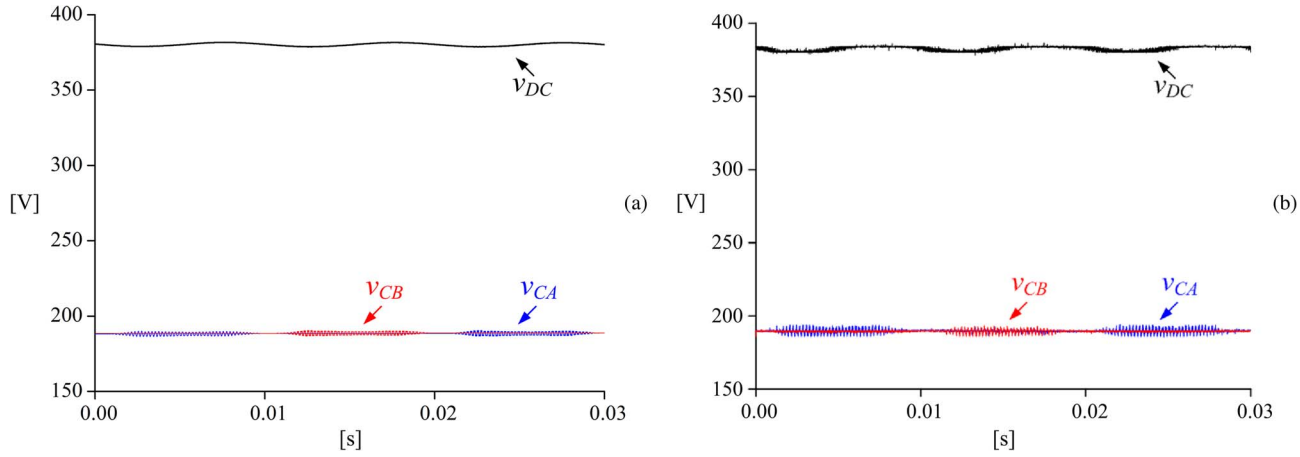

Fig. 11. (Left) Simulation and (right) experimental results: dc bus voltage and FC voltages.

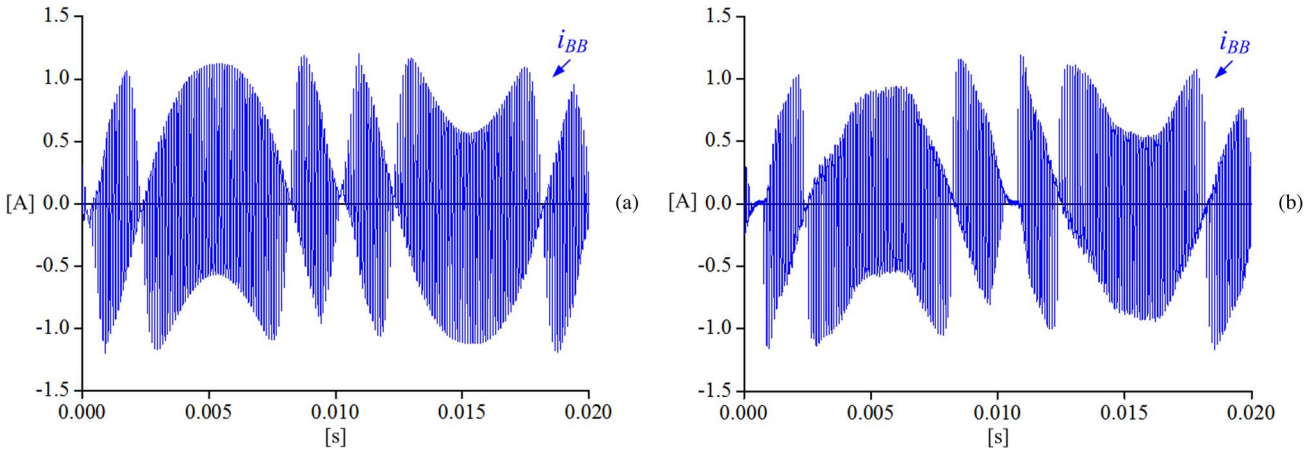

Fig. 12. Balance booster current i_{BB} for (a) simulation and (b) experiment.

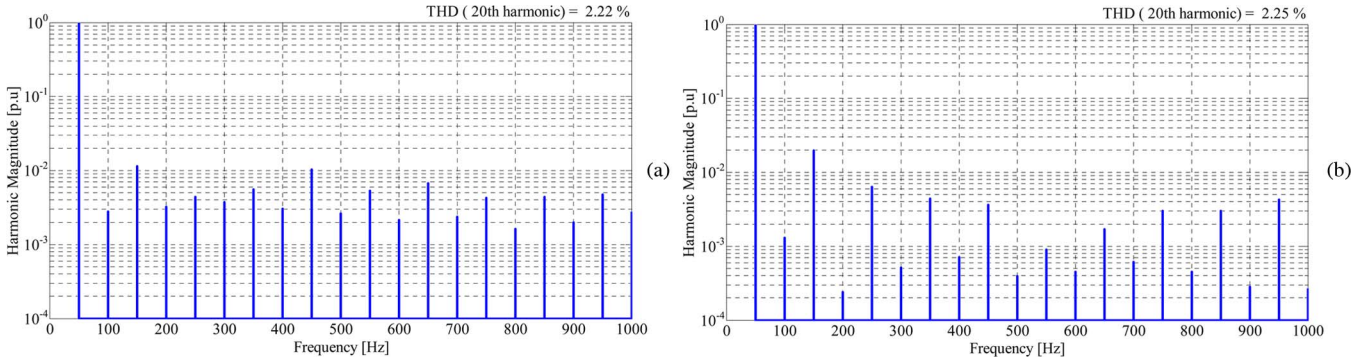

Fig. 13. (Left) Simulation and (right) experimental spectra of grid input current i_{IN}.

The simulation and experimental waveforms for input current i_{IN} are presented in Fig. 10(a) and (b), respectively. Note the very small current ripple and cusp distortion that have been achieved despite the relatively low switching frequency of 5 kHz.

Rectifier switched output voltage v_{AB} is shown in Fig. 10(c) and (d) for simulation and experiment, respectively. These results show the distinct and uniformly spaced five-level switching that is expected to be produced by the semi-bridge FC converter. Note in particular the switching null directly after the zero crossings, which is caused by the converter's topological inability to synthesize a reverse-polarity voltage v_{AB} in relation to the i_{IN} current.

Fig. 11(a) and (b) shows the simulation and experimental waveforms for dc bus voltage v_{DC} and FC voltages v_{CA} and v_{CB}. From these figures, the effectiveness of the balance booster in maintaining the FC voltages almost exactly at $v_{\mathrm{DC}}/2$ can be appreciated. The currents i_{BB} flowing through the balance booster for simulation and experiment are shown in Fig. 12(a) and (b), respectively.

Fig. 13(a) and (b) shows the simulation and experimental spectra for input current i_{IN}, respectively. From these figures, it is shown that despite the relatively large per unit (10%) filter inductance that was used, the low-order input current harmonics (up to the 20th harmonic) are quite small. Fig. 14(a) and (b)

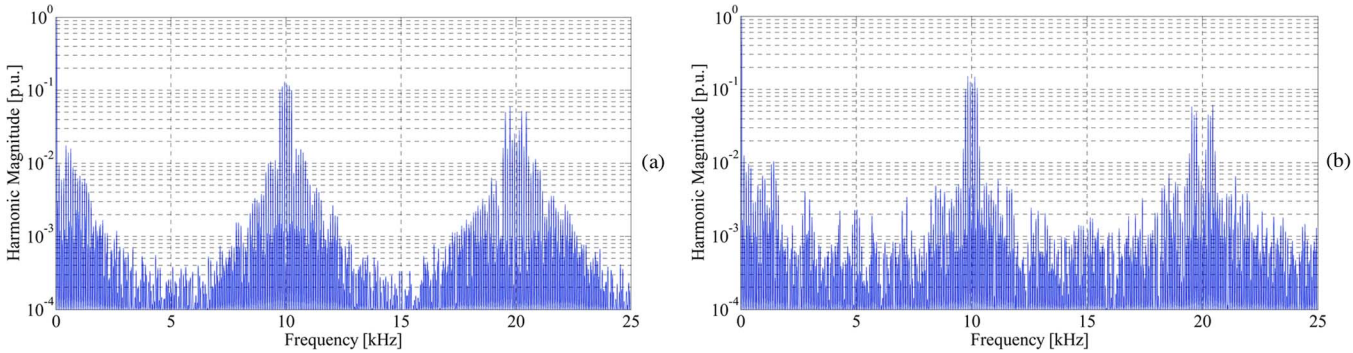

Fig. 14. (Left) Simulation and (right) experimental spectra of rectifier switched output voltage v_{AB}.

shows the simulation and experimental spectra, respectively, for rectifier switching voltage v_{AB}, where the cancelation of the first carrier group harmonics around 5 kHz can be clearly seen as expected.

VIII. Conclusion

This paper has presented a single-phase semi-bridge five-level rectifier structure based on the FC topology. Compared with two-level converters, this new multilevel converter substantially assists the tradeoff between current distortion and switching ripple by canceling the first carrier group harmonics. The FC topology also allows lower voltage-rating devices to be used, with a consequential improvement in converter efficiency.

The converter has been modulated using 180° discontinuous PSC-PWM, with a balance booster circuit included to assist natural balancing of the FC voltages.

The precise agreement that has been achieved between simulation and experiment for all time- and frequency-domain measurements fully validates the theoretical and practical functionalities of this new semi-bridge topology.

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